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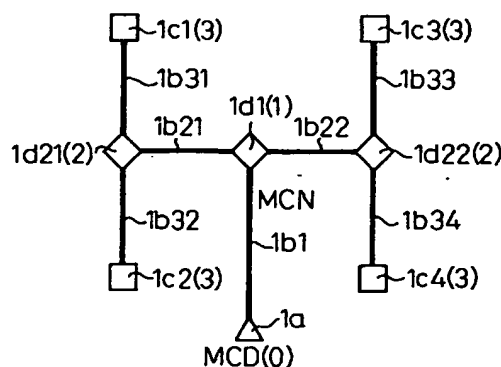
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54 Designing semiconductor integrated circuits.

57 A method of placing and routing elements of a semiconductor integrated circuit picks out a signal net (MCN), a driver (MCD) of the signal net, and load cells driven by the driver among the elements of the integrated circuit, places the driver at a first position, defines a first range based on the first position, determines a second position in the first range, defines a second range based on the second position, and collectively places the load cells of a predetermined number in the second range. Namely, the method deals with a signal net in the integrated circuit, a driver of the net, and load cells driven by the driver. The method sets conditions on the signal net, driver, and load cells, when placing and routing the elements of the integrated circuit, to thereby reduce skew (skew time), wiring overhead, and time delay in the integrated circuit and speedily and easily place and route the elements.

Fig. 6



The present invention relates to designing semiconductor integrated circuits, and in particular methods of apparatus for placing and routing elements of such semiconductor integrated circuits, for example with the use of a computer.

A computer aided design (CAD) system is used to design a semiconductor integrated circuit (IC). This system requires a method of and an apparatus for speedily and easily placing and routing elements of the IC while reducing skew (skew time), wiring overhead, and propagation delay times in the IC.

The prior art adopted for CAD systems first prepares a net list involving various cells, and then routes the cells. This technique is insufficient in various points. Concretely, in the prior art, a time dependent layout technique for placing and routing elements of a semiconductor IC is provided.

For example, in this prior art time dependent layout technique, a very long time is required to complete the placing and routing of a semiconductor IC. Note that the prior art suppresses skew by adjusting load capacitance and by employing balanced wiring, snaking wiring, and star wiring. In addition, the prior art must secure a margin of space to suppress skew. This reduces an available area for logic circuits.

Further, the prior art must artificially induce delays at a high speed terminal (fast terminal) relative to a terminal (slow terminal) that receives a signal behind the high speed terminal, to suppress skew. This increases the overall time delay in producing the IC. An IC production operation usually involves temporal fluctuations due to variations in temperature, processes, and source voltages. These fluctuations affect time delay in the IC. The prior art, therefore, must consider a margin for absorbing such fluctuations.

It is desirable to provide a method of and an apparatus for speedily and easily placing and routing elements of a semiconductor IC while reducing skew (skew time), wiring overhead, and a wiring area in the IC as well as propagation delay times and power consumption of the IC?

In an embodiment of the present invention, there is provided a method of placing and routing elements of a semiconductor integrated circuit, comprising the steps of picking out a signal net, a driver unit of the signal net, and load cells driven by the driver unit among the elements of the integrated circuit; placing the driver unit at a first position, defining a first range based on the first position; fixing a second position in the first range; defining a second range based on the second position; and collectively placing and routing the load cells of predetermined number in the second range.

The first range may be the whole of a first area around the first position, or a range between a first area around the first position and a second area defined in the first area. The method may include the steps of preparing a plurality of second positions and

routing the first position to the plurality of second positions through star wiring. The signal net may be a clock signal net, the driver unit is a clock driver, and the load cells may be flip-flops.

The method may include the step of placing the load cells in a reserved area of predetermined size. The method may include the step of placing the load cells along a reserved line of predetermined length. The method may include the step of placing the load cells along the reserved line with clock terminals of the load cells being positioned along the reserved line, so that the capacitance of a line from a branch point to any one of the load cells may be determined by the length of the line.

The method may include the step of placing the load cells along the reserved line side by side such that short sides of each load cell are in parallel with the reserved line. The method may include the step of placing the load cells like a spine with the reserved line serving as a base line. The method may include the step of replacing load cells on the same reserved line with each other according to associations with respect to peripheral cells. The method may include the step of replacing load cells on different reserved lines with each other according to associations with respect to peripheral cells?

The method may include the step of placing reserved lines in an area that satisfies a target skew with respect to a driver cell. The method may include the step of connecting the reserved lines to the driver cell through star wiring with the driver cell serving as a root. The method may include the step of connecting equipotential output terminals of the driver cell to the reserved lines, respectively.

Further, in another embodiment of the present invention, there is provided an apparatus for placing and routing elements of a semiconductor integrated circuit, having an input unit for entering data, a storage unit for storing data, a processor for placing and routing the elements of the integrated circuit according to data from the input unit and the storage unit, and a display unit for displaying images according to data provided by the processor, wherein the apparatus comprises a unit for picking out a signal net, a driver of the signal net, and load cells connected to the driver among the elements of the integrated circuit; a unit for placing the driver at a first position; a unit for defining a first range based on the first position, fixing a second position in the first range, and defining a second range based on the second position; and a unit for collectively placing and routing the load cells of predetermined number in the second range.

The storage unit may comprise a unit for storing logic circuit information such as a net list; a unit for storing routing attribute information to identify clocks and signals; a unit for storing resource information such as information about the elements of the integrated circuit; and a unit for storing programs such as

sequences of processes. The first range may be the whole of a first area around the first position. The first range may be a range between a first area around the first position and a second area defined in the first area.

A plurality of second positions may be defined, and the first position may be connected to the plurality of second positions through star wiring. The signal net may be a clock signal net, and the load cells may be flip-flops. The load cells may be placed in a reserved area of predetermined size. The load cells may be placed along a reserved line of predetermined length.

The load cells may be placed along the reserved line with the clock terminals of the load cells being positioned along the reserved line, so that the capacitance of a line from a branch point to any one of the load cells may be determined by the length of the line. The load cells may be placed along the reserved line side by side such that short sides of each load cell are in parallel with the reserved line. The load cells may be placed like a spine with the reserved line serving as a base line.

Load cells on the same reserved line may be replaced with each other according to associations with respect to peripheral cells. Load cells on different reserved lines may be replaced with each other according to associations with respect to peripheral cells. Reserved lines may be placed in an area that satisfies a target skew with respect to the driver cell. The reserved lines may be connected to the driver cell through star wiring with the driver cell serving as a root. The driver cell may have output terminals of the same potential, which are connected to the reserved lines, respectively.

According to an embodiment of another aspect of the present invention, there is also provided a semiconductor integrated circuit, characterized in that a signal net and load cells connected to the signal net are picked out from elements of the integrated circuit, and that the load cells are placed and routed in a reserved area of predetermined size.

The signal net may be a clock signal net, and the load cells may be flip-flops. The load cells may be placed along a reserved line of predetermined length. A branch point may be defined in a first range around a position of a clock buffer, and the load cells of predetermined number may be collectively placed in a second range that is defined according to the branch point.

The load cells may be placed such that clock terminals of the load cells are arranged along the reserved line. The load cells may be placed along the reserved line side by side such that the short sides of each load cell are in parallel with the reserved line. The load cells may be placed like a spine with the reserved line serving as a base line.

A plurality of reserved lines may be placed in an

area that satisfies a target skew with respect to the driver cell. The reserved lines may be connected to the driver cell through star wiring with the driver cell serving as a root. The driver cell may have output terminals of the same potential, which are connected to the reserved lines, respectively.

One embodiment of the present invention can provide a method of placing and routing elements of a semiconductor integrated circuit by picking out a signal net from the elements of the integrated circuit and routing the signal net, wherein the method comprises the step of extending or shortening end lines if one end line is extended or shortened.

The method may include the step of extending or shortening end lines in response to a change in a capacitance or resistance of a line.

Further, another embodiment of the present invention can provide a method of placing and routing elements of a semiconductor integrated circuit by picking out a signal net from the elements of the integrated circuit and routing the signal net, wherein the method comprises the step of branching an end line if another end line is branched.

The signal net may be a clock signal net. The method may include the step of routing the signal net along a reserved area. The method may include the step of calculating arrival time at each predetermined position in the signal net.

The method may include the step of determining a width of each line in the signal net so as to minimize the arrival time calculated at each predetermined position. The method may include the step of displaying the calculated arrival time in the vicinity of each predetermined position on a screen that displays the signal net. The predetermined positions in the signal net may include branch points and end points of the signal net.

A further embodiment of the present invention can also provide an apparatus for placing and routing elements of a semiconductor integrated circuit, having an input unit for entering data, a storage unit for storing data, a processor for placing and routing the elements of the integrated circuit according to data from the input unit and the storage unit, and a display unit for displaying images according to data provided by the processor, wherein the apparatus comprises a unit for picking out a signal net among the elements of the integrated circuit; a unit for extending or shortening one of end lines when routing the signal net; and a unit for extending or shortening the other end lines in response to the extension or shortening of the end line.

The end lines may be extended or shortened in response to a change in a capacitance or resistance of a line.

In addition, an embodiment of the present invention can provide an apparatus for placing and routing elements of a semiconductor integrated circuit, hav-

ing an input unit for entering data, a storage unit for storing data, a processor for placing and routing the elements of the integrated circuit according to data from the input unit and the storage unit, and a display unit for displaying images according to data provided by the processor, wherein the apparatus comprises a unit for picking out a signal net among the elements of the integrated circuit; a unit for branching one of end lines when routing the signal net; and a unit for branching another end line in response to the branching of the end line.

The storage unit may comprise a unit for storing logic circuit information such as a net list; a unit for storing routing attribute information to identify clocks and signals; a unit for storing resource information such as information about the elements of the integrated circuit, and a unit for storing programs such as sequences of processes. The signal net may be a clock signal net. The signal net may be routed along a reserved area.

An arrival time at a predetermined position in the signal net may be calculated. A width of each line in the signal net may be determined to minimize the arrival time calculated at each predetermined position. The calculated arrival time may be displayed in the vicinity of each predetermined position on a screen that displays the signal net. The predetermined positions in the signal net may include branch points and end points of the signal net.

Reference will now be made, by way of example, to the accompanying drawings, wherein:

Fig. 1 is a flowchart showing the steps of placing and routing elements of a semiconductor IC according to a prior art method;

Fig. 2 explains the principle of a method of placing and routing elements of a semiconductor IC embodying the present invention;

Fig. 3 explains a process of defining modules of a semiconductor IC embodying the present invention;

Fig. 4 explains a process of securing an area for a main clock net of an IC embodying the present invention;

Fig. 5 explains a process of automatically routing the main clock net embodying the present invention;

Fig. 6 shows a net displayed on a screen in a process embodying a first aspect of the present invention;

Fig. 7 shows a process of extending and shortening lines embodying the first aspect of the present invention;

Fig. 8 shows another process of extending and shortening lines embodying the first aspect of the present invention;

Fig. 9 shows still another process of extending and shortening lines embodying the first aspect of the present invention;

Fig. 10 shows a process of branching a line embodying the first aspect of the present invention; Fig. 11 shows an example of predetermined routes in a process embodying the first aspect of the present invention;

Fig. 12 shows calculations of arrival time of a signal in a process embodying the first aspect of the present invention;

Fig. 13 shows arrival time of a signal in a process embodying the first aspect of the present invention;

Fig. 14 explains a process of placing local clock drivers of the IC embodying the present invention;

Fig. 15 explains a process of routing a global clock net of the IC embodying the present invention;

Fig. 16 explains a process of securing an area for placing flip-flops of the IC embodying the present invention;

Fig. 17 explains a process of initially placing flip-flops of the IC embodying the present invention; Fig. 18 explains a process of automatically placing elements of the IC embodying the present invention;

Fig. 19 explains a block of target cells arranged along a reserved line embodying a second aspect of the present invention;

Fig. 20 shows blocks of target cells in a process embodying the second aspect of the present invention;

Fig. 21 shows the position of a clock terminal in a target cell in a process embodying the second aspect of the present invention;

Fig. 22 shows an improvement in an arrangement of target cells in a block according to the second aspect of the present invention;

Fig. 23 shows an improvement in an arrangement of blocks of target cells according to the second aspect of the present invention;

Fig. 24 shows an allowable area for placing blocks of target cells in a process embodying the second aspect of the present invention;

Fig. 25 shows a line in a block of target cells according to the second aspect of the present invention;

Fig. 26 shows lines between a driver and blocks of target cells according to the second aspect of the present invention;

Fig. 27 explains output terminals of a driver cell according to the second aspect of the present invention;

Fig. 28 shows lines between a driver and blocks of target cells according to the second aspect of the present invention;

Fig. 29 is a flowchart showing the steps of placing and routing elements of a semiconductor IC in a process embodying the present invention; and

Figs. 30A and 30B are general views showing a method of and an apparatus for placing and routing elements of a semiconductor IC embodying the present invention.

For a better understanding of the preferred embodiments of the present invention, the problems of a prior art will be explained.

A CAD system is used to place and route elements of a master slice semiconductor IC such as a gate array and a standard cell. The prior art adopted for the CAD system first prepares a net list involving various cells and then routes the cells. This technique is insufficient in various points.

Figure 1 is a flowchart showing the steps of placing and routing elements of a semiconductor IC according to the prior art. This is called a Timing Driven Layout technique.

Step ST1 designs a system or a board. Step ST2 designs chips or blocks. Step ST3 logically synthesizes each block, or manually designs each block. Step ST4 designs gates, or prepares a net list. The steps ST1 to ST4 are in a logic design phase.

Step ST5 places I/O cells, RAMs, multipliers, etc., determines the sizes and positions of blocks, roughly places and routes gates, and tests the degree of congestion, which is called as a floor plan in this specification. Step ST6 manually places and routes some elements. Step ST7 automatically places elements, and step ST8 automatically routes the elements.

Step ST9 extracts a given cell out of the IC, i.e., a chip whose elements have been placed and routed. Step ST10 calculates a delay in the arrival time of a signal and simulates the operation of the chip. The delay time and simulation results provided by the step ST9 are fed back to the steps ST1 to ST4 to repeat these steps. The extraction process in the step ST9 is also carried out in the steps ST6 and ST7.

The Timing Driven Layout technique must repeat these steps, for example, three times, and it takes about one month, until the step ST8 first carries out the automatic routing process. Accordingly, the prior art takes a very long time to complete the placing and routing of a semiconductor IC.

The prior art suppresses skew by adjusting load capacitance and by employing balanced wiring, snaking wiring, and star wiring. In addition, the prior art must secure a margin space to suppress skew. This reduces the available area for logic circuits. The prior art must prolong delay at a fast terminal relative to a slow terminal that receives a signal behind the fast terminal, to suppress skew. This increases propagation delay times in the IC as a whole. An IC operation usually involves temporal fluctuations due to variations in temperature, processes, and source voltages. These fluctuations affect time delay in the IC. The prior art, therefore, must consider a time margin (waste time) for absorbing such fluctuations.

The principle of a method of placing and routing

elements of a semiconductor IC embodying the present invention will be explained next with reference to Fig. 2.

One embodiment of the present invention deals with, among elements of the IC, a signal net, a driver of the net, and load cells (flip-flops) driven by the driver. The present invention places the driver at a first position, sets a first range (area) based on the first position, determines a second position in the first range, fixes a second range based on the second position, and collectively arranges the load cells in the second range.

In an example, the signal net is a clock signal net, the driver is a clock driver or a clock buffer, and the load cells are flip-flops.

In this way, the present invention picks out a signal net, a driver or a clock buffer of the net, and load cells connected to the net among elements of a semiconductor IC. The present invention places the driver at a first position, sets a first range based on the first position, determines a second position in the first range, fixes a second range based on the second position, and collectively arranges the load cells in the second range.

The present invention speedily and easily places and routes elements of a semiconductor IC while minimizing skew (skew time), wiring overhead, and propagation delay times in the IC.

Methods and apparatuses for placing and routing elements of a semiconductor IC according to the embodiments of the present invention will be explained next with reference to the drawings.

Figures 3 to 5 and 14 to 18 show examples of images displayed by a CAD system employing a method embodying the present invention. Figures 6 to 13 explain the first aspect of the present invention shown in Figs. 3 to 5. Figures 19 to 28 explain the second aspect of the present invention shown in Figs. 14 to 18.

More precisely, Fig. 3 shows a process of setting module areas, Fig. 4 shows a process of securing an area for a main clock net, and Fig. 5 shows a process of automatically routing the main clock net. In these figures, a chip overview window 11 generally displays a chip, an operation board window 12 displays specified operations, a chip window 13 displays placed and routed elements of the chip, a net schema window 14 displays net information, and a main clock control panel window 15 displays main clock control information.

In Figs. 3 to 5, the chip 101 includes module areas 111 to 116 and layout blocks 110a to 110n for memories, etc. The chip 101 corresponds to a master slice semiconductor IC such as a gate array or a standard cell. The periphery of the chip 101 involves I/O terminals 120 and I/O circuits 130.

In Fig. 3, the module areas are first determined. There are six module areas 111 to 116. Laid-out blocks are read and placed in the modules. Namely,

the 14 laid-out blocks 110a to 110n are copied onto the chip 101. Instead of copying the blocks, previously used layout data of blocks may be reused. The process of laying out blocks may be carried out later, for example, after the process of securing an area for a main clock net.

In Fig. 4, an area for a main clock net MCN is secured. A reference mark 0 is an output terminal of a main clock driver MCD 130a, W is a bend, 1 and 2 are branch points, and 3 is an end point of the main clock net. The main clock driver 130a has an I/O terminal 120a. Each of the bends W, branch points 1 and 2, and end points 3 is displayed with estimated delay time in the main clock net.

Global clock drivers GCD to be placed are displayed in the net schema window 14, and they are properly assigned to the end points 3, respectively, as shown in Fig. 5. The global clock drivers may be placed at the bends W and branch points 1 and 2.

In Fig. 5, the main clock net MCN is automatically routed in the area secured as mentioned above. The global clock drivers GCD are placed at the end points 3, respectively. The main clock net MCN includes nets MCN1 and MCN2. The net MCN1 is indicated with a dotted line and extends from the output terminal 0 of the main clock driver 130a to the first branch point 1. The net MCN1 is made of a thick wire. The net MCN2 is indicated with a continuous line and extends from the first branch point 1 to the respective global clock drivers. The net MCN2 is made of a wire of normal width.

Line delay between the output terminal 0 of the main clock driver 130a to the input point of each global clock driver and the skew of the main clock net are displayed in the net schema window 14 of Fig. 5. The lower left end point in Fig. 5 is connected to two global clock drivers, to produce a larger line delay (phase delay) than the other end points. While the main clock net is being automatically routed, placing of elements is prohibited to prevent a short circuit in later processes.

The processes of Figs. 3 to 5 according to the first aspect of the present invention will be explained next with reference to Figs. 6 to 13.

Figure 6 shows an example of a main clock net MCN.

The main clock net includes a start point 1a, lines 1b1, 1b21, 1b22, 1b31, 1b32, 1b33, and 1b34, end points 1c1, 1c2, 1c3, and 1c4, and branch points 1d1, 1d21, and 1d22. The start point 1a corresponds to the output terminal 0 of the main clock driver 130a, the lines 1b1, 1b21, 1b22, 1b31, 1b32, 1b33, and 1b34 correspond to the lines of the nets MCN1 and MCN2, the end points 1c1, 1c2, 1c3, and 1c4 correspond to the end points 3, and the branch points 1d1, 1d21, and 1d22 correspond to the branch points 1 and 2.

Figure 7 shows an example of a process of extending and shortening a line according to the first as-

pect of the present invention. Figures 8 and 9 show other processes of extending and shortening a line. The first aspect of the present invention deals with a clock net between a main clock driver and end points, and the second aspect of the present invention deals with a reserved line between a local clock driver and flip-flops.

In Fig. 7, a cursor 2c in the chip window 13 on the display is manipulated to move an end point 2b1. According to the movement of the end point 2b1, the other end point 2b2 also moves in an extending or shortening direction. When a line 2a1 from a branch point 1d1 to the end point 2b1 in the main clock net is extended, a line 2a2 from the branch point 1d1 to the other end point 2b2 is extended by a length equal to the extension in the line 2a1. On the other hand, when the line 2a1 is shortened, the line 2a2 is also shortened accordingly. Irrespective of the expansion or shortening in the line 2a1, a line 1b1 from the output terminal 1a of the main clock driver to the branch point 1d1 is unchanged.

Figure 8 involves three end points 2b1, 2b2, and 2b3, instead of the two end points 2b1 and 2b2 of Fig. 7. When the cursor 2c is manipulated to move the first end point 2b1, the end points 2b2 and 2b3 are moved accordingly. Namely, when a line 2a1 from a branch point 1d1 to the end point 2b1 in the main clock net is extended, a line 2a2 from the branch point 1d1 to the end point 2b2 and a line 2a3 from the branch point 1d1 to the end point 2b3 are also extended by the extension in the line 2a1. Similarly, when the line 2a1 is shortened, the lines 2a2 and 2a3 are shortened accordingly. Irrespective of the extension or shortening in the line 2a1, a line 1b1 from the output terminal 1a of the main clock driver to the branch point 1d1 is unchanged.

In this way, lines from a branch point to end points are extended or shortened according to an expansion or a shortening in one line, so that the lines from the output terminal 1a to the end points 2b1, 2b2, 2b1, 2b2, and 2b3 may have identical delay times in transmitting a clock signal.

Figure 9 shows lines 2a1 and 2a2 of different lengths. When the cursor 2c is manipulated to move an end point 2b1, the other end point 2b2 is extended or shortened according to a change in line capacitance or line resistance due to the movement of the end point 2b1. Namely, when the line 2a1 is extended or shortened, the line 2a2 is extended or shortened according to a change in the capacitance or resistance of the line 2a1, so that a change in the capacitance or resistance of the line 2a2 may correspond to the change in the capacitance or resistance of the line 2a1.

Even if the widths of lines from a branch point to end points differ from one another, one of the lines may be extended or shortened according to a change in the capacitance or resistance of another that has

been extended or shortened. As a result, the lines from the output terminal 1a of the main clock driver to the end points 2b1 and 2b2 may have identical delay times for transmitting a signal.

Figure 10 shows a process of branching a line according to the first aspect of the present invention. This example branches an end point into two end points.

Namely, an end point 2b1 is divided into two end points 1c1 and 1c2. If required at this time, an instruction may be issued to branch the other end point 2b2 into two end points 1c3 and 1c4. In this case, the lengths of lines 1b33 and 1b34 between the branch point 1d22 (2b2) and the end points 1c3 and 1c4 correspond to the lengths of lines 1b31 and 1b32 between the branch point 1d21 (2b1) and the end points 1c1 and 1c2. Similar to the embodiment of Fig. 9, the length of each line is determined according to a change in the capacitance or resistance of a line that has been extended or shortened, if the lines have different widths.

As a result, lines from the output terminal 1a of the main clock driver to the end points 1c1, 1c2, 1c3, and 1c4 have identical delay times for transmitting a signal, even if the lines are branched. This makes the designing of branches easier.

Figure 11 shows a predetermined routing area. For example, the lines from the output terminal 1a of the main clock driver to the four end points 1c1, 1c2, 1c3, and 1c4 in the main clock net are routed in the predetermined area PDA of Fig. 11. The wiring area PDA is reserved for routing lines. This technique is advantageous in calculating the range of delay to occur when transmitting a signal through the lines to be laid in the area PDA.

Figure 12 shows calculations of arrival time of a signal. A reference mark  $T_{arrival}(n)$  is arrival time at a branch point or end point  $n$ ,  $C_{effect}(n)$  is line capacitance at the point  $n$ , and  $C_{load}(n)$  is line resistance at the point  $n$ .  $R_{line}(n)$  and  $C_{line}(n)$  are resistance and capacitance values calculated according to the length of a line between branch points, or between a branch point and an end point.

According to the first aspect of the present invention, delay (arrival time) calculated as shown in Fig. 12 is displayed in the vicinity of the corresponding branch or end point. The arrival time of a clock signal at a branch or end point may be calculated according to a known technique.

Figure 13 shows signal arrival time (delay) at each of the branch points and end points in the main clock net of Fig. 6 displayed in the chip window 13. In the window 13, an operator may confirm the delay time at each branch or end point before actually routing the main clock net. The width of each line of the main clock net may be automatically determined to minimize the delay time at each branch or end point.

As explained above, the first aspect of the pres-

ent invention is capable of optimizing the layout of a semiconductor IC through interactive operations. The first aspect of the present invention provides information for reducing skew and supports layout work. Consequently, the first aspect of the present invention improves the performance of the IC and the efficiency of the layout work.

Figure 14 explains a process of placing local clock drivers in a semiconductor IC, Fig. 15 explains a process of routing a global clock net, Fig. 16 explains a process of setting an area for placing flip-flops, Fig. 17 explains a process of initially placing the flip-flops, and Fig. 18 explains a process of automatically placing elements of the IC, according to the second aspect of the present invention. Throughout the figures, a global clock control panel window 16 displays global clock control information, and a local clock control panel window 17 displays local clock control information.

In Fig. 14, local clock drivers (LCDs) are placed after the automatic routing of the main clock net of Fig. 5. The local clock drivers may be automatically placed uniformly in a module area. If the automatically placed drivers are not satisfactory, they may be adjusted.

Figure 14 shows five local clock drivers. In the chip window 13 of Fig. 14, the local clock drivers are shown connected to a global clock driver (GCD) with dotted lines because they are not routed yet. Namely, a net shown in the chip schema window 14 is not completed yet, and therefore, the net is indicated with the dotted lines in the chip window 13.

In Fig. 15, the global clock net is routed, i.e., the global clock driver is routed to the local clock drivers. To suppress skew, the global clock driver is directly connected to the local clock drivers. At this time, line delay and skew between the output of the global clock driver and the inputs of the local clock drivers are displayed in the net schema window 14. During this process, placing elements is prohibited to prevent a short circuit in later processes. The global clock net may be equidistantly routed to suppress skew. Figures 14 and 15 show the chip window 13, net schema window 14, and global clock control panel window 16.

In Fig. 16, guide lines, i.e., reserved lines (FFbar) are set to efficiently place flip-flops. The flip-flops are placed along each reserved line such that the bottom of each flip-flop is on the reserved line. This arrangement minimizes wiring because each flip-flop has a clock terminal at the bottom thereof. The number of flip-flops allocated is equal to the number of reserved lines, to equalize the capacitance of the reserved lines. This enables the skew of the net to be controlled by only adjusting distances from the local clock drivers to the reserved lines.

In the local clock control panel window 17 of Fig. 16, a parameter "Cells/FFbar" indicates the number of one-bit flip-flops on a reserved line FFbar, "Stub

Length" indicates a maximum line length from a reserved line FFbar to flip-flops, "FFbar Length" indicates the maximum length of a reserved line, and "Root Net Length" indicates a maximum line length from a local clock driver to a reserved line FFbar. In the chip window 13, a diamond indicated with a dotted line represents the maximum length of a root net. If the center of a reserved line is out of the diamond, a skew larger than an estimated value will occur. In Fig. 16, there are three reserved lines.

In Fig. 17, the flip-flops are automatically placed along each reserved line. Cells connected to a local clock net (LCN) are recognized as flip-flops, and the cells are uniformly allocated for reserved lines. Accordingly, any cells including flip-flops are routed with low skew. Thereafter, the cells are annealed. The annealing will be explained later in detail. At this time, the flip-flops are moved along the respective reserved lines, to maintain estimated skew. It is possible to exchange the flip-flops with one another among the reserved lines. The net schema window 14 is used to confirm line delay and skew between the output of each local clock driver to the flip-flops. If the flip-flops are exchanged with one another, the skew will change.

In Fig. 18, cells not yet placed are automatically placed and traded. In the chip window 13 of Fig. 18, hatched cells are flip-flops driven by local clock drivers. The flip-flops may be annealed on the respective reserved lines. At this time, routes between the local clock drivers and the flip-flops are fixed. Since the flip-flops are lined up as shown in Fig. 18, channels occupied by the local clock net will be minimized. Due to the small amount of skew, a timing fault will not occur. To prevent a timing fault, the following must be satisfied:

$$\text{skew time (skew)} < (\text{transmission time of flip-flops} + \text{transmission time between flip-flops} - \text{hold time of flip-flops})$$

Figure 19 shows a block of target cells placed along a reserved line, Fig. 20 shows blocks of target cells, and Fig. 21 shows the position of a clock terminal in a target cell, according to the second aspect of the present invention.

In Fig. 19, a reserved line FFbar is set to efficiently place target cells, i.e., flip-flops along the reserved line. The target cells form a block 140 corresponding to a reserved area.

Figure 20 shows blocks 140 of target cells. The size of each block 140 is predetermined. Namely, the range of delay time in each block 140 is known. The clock terminal of each target cell is at the bottom thereof as shown in Fig. 21. When the bottom of each target cell is positioned along the reserved line as shown in Fig. 19, no waste wiring will be formed.

Figure 22 shows a process of improving the arrangement of target cells in each block, and Fig. 23 shows another process of improving the arrange-

ment of target cells among blocks, according to the second aspect of the present invention. These processes are the annealing mentioned in connection with Fig. 17.

In Fig. 22, a cell (flip-flop) B in a block 140 is associated with a peripheral cell 150b, and a cell F in the block 140 is associated with a peripheral cell 150a. These cells in the block 140 are rearranged to shorten routes. Namely, the cells B and F are replaced with each other. Since the cells B and F are on the same reserved line, they are included in the range of delay time of the reserved line.

In Fig. 23, a cell (flip-flop) E in a block 140a is associated with a peripheral cell 150d, and a cell K in a block 140b is associated with a peripheral cell 150c. In this case, the cell E in the block 140a on a reserved line FFbar1 is replaced with the cell K in the block 140b on a reserved line FFbar2, to shorten routes.

Figure 24 shows an allowable area for placing blocks of target cells. Namely, blocks 140c, 140d, 140e, and 140f of target cells are placed in a diamond area such as a Manhattan Diamond area SS so that the blocks satisfy a target skew with respect to a driver cell, i.e., a local clock driver LCD. The driver cell LCD may be connected to the blocks 140c to 140f through star wiring, so that the range of delay time in these blocks is calculable. Namely, the skew of target cells in each block may be limited within a predetermined range.

The area for placing the blocks 140c to 140f of target cells may be between an outer area SS and an inner area SS'. This technique sets the upper and lower limits of the range of delay time of blocks. The number of the blocks of target cells may be at least one.

Figure 25 shows routes of target cells in a block and Fig. 26 shows routes between a driver and blocks of target cells, according to the second aspect of the present invention.

In Fig. 25, a reserved line FFbar serves as a base line along which flip-flops are placed like a spine. The terminal of a driver is not shown.

In Fig. 26, a driver LCD is connected to blocks 140c to 140f of target cells through star wiring with the driver serving as a root, so that the range of delay time of the blocks is known in advance.

Figure 27 explains output terminals of a driver cell, and Fig. 28 shows routes between a driver and blocks of target cells.

In Fig. 27, the output terminals of the driver cell, i.e., the local clock driver (LCD) have the same potential and different terminal definitions. Accordingly, the output terminals of the driver cell may be connected to the blocks of target cells, respectively, to realize star wiring.

In this way, the second aspect of the present invention is capable of reducing skew, line delay, route lengths, and a wiring area, to improve circuit integration. The second aspect is also capable of reducing

the capacitance and resistance of wiring and power consumption, improving an operation speed, and minimizing faults due to electromigration.

Figure 29 is a flowchart showing the steps of placing and routing elements of a semiconductor IC in a method embodying the present invention.

Step ST11 designs a system or a board. Step ST12 designs chips. Step ST13 designs blocks. Step ST14 is characteristic to the present invention and synthesizes a main clock tree.

Step ST15 carries out the sizing and placing of blocks (Fig. 3), the placing of main clocks (Figs. 4 to 13), the placing of local clocks (Figs. 14 to 28), and the extracting and analyzing of timing, which is called as a higher floor plan in this specification. The step ST15 prepares clock net information, which is used by the step ST13 to design blocks. The step ST15 also prepares clock layout information, which is used by step ST18 to automatically place elements.

After the step ST13, step ST16 synthesizes data and manually designs elements. Step ST17 designs gates. Step ST18 automatically places the elements, and step ST19 automatically routes the elements.

Step ST20 extracts predetermined cells out of the IC (chip) that has been placed and routed. Step ST21 calculates delay, i.e., signal arrival time and simulates the operation of the circuit. Results of the calculation and simulation are fed back to the steps ST11 to ST14, to change the conditions of these steps.

Compared with the prior art of Fig. 1, the steps ST13 to ST15 deal with clock signal nets such as main clock nets, global clock nets, and local clock nets and flip-flops connected to the clock signal nets, and prepare reserved lines along which the flip-flops are placed. Consequently, the present invention reduces skew, wiring overhead, and time delay in an IC, and speedily and easily places and routes elements of the IC.

Figures 30A and 30B are block diagrams generally showing a CAD system employing a method of placing and routing elements of a semiconductor IC embodying the present invention, in which Fig. 30A is a general view of the CAD system and Fig. 30B shows the functions of a storage unit of the CAD system.

In Fig. 30A, the CAD system includes an input unit 201, a display unit 202, a storage unit 203, and a processor 204. The input unit 201 includes a keyboard, a mouse, a tablet, etc., to be handled by an operator to place and route elements of a semiconductor IC. The display unit 202 displays various images as shown in Figs. 3 to 5 and 14 to 18, so that the operator may interactively place and route the elements of the IC on the display unit 202. The processor 204 carries out processes according to instructions and data entered through the input unit 201 and information read out of the storage unit 203, and successively displays images on the display unit 202.

In Fig. 30B, the storage unit 203 stores logic circuit information 231 such as a net list, routing attribute information 232 for identifying clocks and signals, resource information 233 about chip elements such as physical patterns and terminals, and programs 234 indicating process sequences such as placing and routing sequences.

Embodiments of the present invention are applicable not only to clock signal nets but also to various nets that involve the problems of skew, wiring overhead, and delay.

As explained above in detail, a method of and/or apparatus for placing and routing elements of a semiconductor IC embodying the present invention deal with a given signal net in a semiconductor IC, a driver of the net, and load cells driven by the driver. The present invention sets conditions on the signal net, driver, and load cells when placing and routing the elements of the IC, to thereby reduce skew, wiring overhead, and time delay in the IC and speedily and easily place and route the elements.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.

## Claims

1. A method of placing and routing elements of a semiconductor integrated circuit, comprising the steps of:

picking out a signal net, a driver means of said signal net, and load cells (FF) driven by said driver means among the elements of said integrated circuit;

placing said driver means at a first position, defining a first range based on said first position;

fixing a second position in said first range; defining a second range based on said second position, and

collectively placing and routing the load cells of predetermined number in said second range.

2. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 1, wherein said first range is the whole of a first area around said first position.

3. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 1, wherein said first range is a range between a first area around said first position and

a second area defined in said first area.

4. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 1, 2 or 3, wherein said method includes the steps of preparing a plurality of second positions and routing said first position to said plurality of second positions through star wiring.
5. A method of placing and routing elements of a semiconductor integrated circuit as claimed in any preceding claim, wherein said signal net is a clock signal net, said driver means is a clock driver, and said load cells are flip-flops.
6. A method of placing and routing elements of a semiconductor integrated circuit as claimed in any preceding claim, wherein said method includes the step of placing said load cells in a reserved area (140) of predetermined size.
7. A method of placing and routing elements of a semiconductor integrated circuit as claimed in any preceding claim, wherein said method includes the step of placing said load cells along a reserved line (FFbar) of predetermined length.
8. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 7, wherein said method includes the step of placing said load cells along said reserved line with clock terminals of said load cells being positioned along said reserved line, so that the capacitance of a line from a branch point to any one of said load cells is determined by the length of said line.
9. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 8, wherein said method includes the step of placing said load cells along said reserved line side by side such that short sides of each load cell are in parallel with said reserved line.
10. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 8, wherein said method includes the step of placing said load cells like a spine with said reserved line serving as a base line.
11. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 8, wherein said method includes the step of replacing load cells (B, F) on the same reserved line with each other according to associations with respect to peripheral cells (150a, 150b).
12. A method of placing and routing elements of a

semiconductor integrated circuit as claimed in claim 8, wherein said method includes the step of replacing load cells (E, K) on different reserved lines (FFbar1, FFbar2) with each other according to associations with respect to peripheral cells (150c, 150d).

13. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 7, wherein said method includes the step of placing reserved lines in an area (SS) that satisfies a target skew with respect to a driver cell (LCD).
14. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 13, wherein said method includes the step of connecting the reserved lines to said driver cell through star wiring with said driver cell serving as a root.
15. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 13, wherein said method includes the step of connecting equipotential output terminals of said driver cell to said reserved lines, respectively.
16. An apparatus for placing and routing elements of a semiconductor integrated circuit, having an input unit (201) for entering data, a storage unit (203) for storing data, a processor (204) for placing and routing the elements of said integrated circuit according to data from said input unit and said storage unit, and a display unit (202) for displaying images according to data provided by said processor, wherein said apparatus comprises:
  - a means for picking out a signal net, a driver of said signal net, and load cells connected to said driver among the elements of said integrated circuit;
  - a means for placing said driver at a first position;
  - a means for defining a first range based on said first position, fixing a second position in said first range, and defining a second range based on said second position; and
  - a means for collectively placing and routing said load cells of predetermined number in said second range.
17. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 16, wherein said storage unit (203) comprises:
  - a means (231) for storing logic circuit information such as a net list;

a means (232) for storing routing attribute information to identify clocks and signals;

a means (233) for storing resource information such as information about the elements of said integrated circuit; and

a means (234) for storing programs such as sequences of processes.

18. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 16, wherein said first range is the whole of a first area around said first position. 10
19. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 16, wherein said first range is a range between a first area around said first position and a second area defined in said first area. 15
20. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in any one of claims 16 to 19, wherein a plurality of second positions are defined, and said first position is connected to said plurality of second positions through star wiring. 20
21. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in any one of claims 16 to 20, wherein said signal net is a clock signal net, and said load cells are flip-flops. 25
22. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in any one of claims 16 to 21, wherein said load cells are placed in a reserved area (140) of predetermined size. 30
23. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in any one of claims 16 to 22, wherein said load cells are placed along a reserved line (FFbar) of predetermined length. 40
24. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 23, wherein said load cells are placed along said reserved line with the clock terminals of said load cells being positioned along said reserved line, so that the capacitance of a line from a branch point to any one of said load cells is determined by the length of said line. 45
25. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 24, wherein said load cells are placed along said reserved line side by side such that short sides of each load cell are in parallel with said re- 50

served line.

26. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 24, wherein said load cells are placed like a spine with said reserved line serving as a base line. 5
27. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 24, wherein load cells (B, F) on the same reserved line are replaced with each other according to associations with respect to peripheral cells (150a, 150b). 10
28. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 24, wherein load cells (E, K) on different reserved lines (FFbar1, FFbar2) are replaced with each other according to associations with respect to peripheral cells (150c, 150d). 15
29. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 23, wherein reserved lines are placed in an area (SS) that satisfies a target skew with respect to said driver cell (LCD). 20
30. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 29, wherein said reserved lines are connected to said driver cell through star wiring with said driver cell serving as a root. 25
31. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 29, wherein said driver cell has output terminals of the same potential, which are connected to said reserved lines, respectively. 30
32. A semiconductor integrated circuit, characterized in that a signal net and load cells connected to said signal net are picked out from elements of said integrated circuit, and that said load cells are placed and routed in a reserved area (140) of predetermined size. 35
33. A semiconductor integrated circuit as claimed in claim 32, wherein said signal net is a clock signal net, and said load cells are flip-flops. 40
34. A semiconductor integrated circuit as claimed in claim 32 or 33, wherein said load cells are placed along a reserved line (FFbar) of predetermined length. 45
35. A semiconductor integrated circuit as claimed in claim 34, wherein a branch point is defined in a 50

first range around a position of a clock buffer, and said load cells of predetermined number are collectively placed in a second range that is defined according to said branch point.

36. A semiconductor integrated circuit as claimed in claim 35, wherein said load cells are placed such that clock terminals of said load cells are arranged along said reserved line.
37. A semiconductor integrated circuit as claimed in claim 36, wherein said load cells are placed along said reserved line side by side such that the short sides of each load cell are in parallel with the reserved line.
38. A semiconductor integrated circuit as claimed in claim 36, wherein said load cells are placed like a spine with said reserved line serving as a base line.
39. A semiconductor integrated circuit as claimed in claim 34, wherein a plurality of reserved lines are placed in an area (SS) that satisfies a target skew with respect to said driver cell (LCD).
40. A semiconductor integrated circuit as claimed in claim 39, wherein said reserved lines are connected to said driver cell through star wiring with said driver cell serving as a root.
41. A semiconductor integrated circuit as claimed in claim 39, wherein said driver cell has output terminals of the same potential, which are connected to said reserved lines, respectively.
42. A method of placing and routing elements of a semiconductor integrated circuit by picking out a signal net from the elements of said integrated circuit and routing said signal net, wherein said method comprises the step of extending or shortening end lines (2a2; 2a2, 2a3) if one end line (2a1) is extended or shortened.
43. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 42, wherein said method includes the step of extending or shortening end lines (2a1, 2a2) in response to a change in a capacitance or resistance of a line.
44. A method of placing and routing elements of a semiconductor integrated circuit by picking out a signal net from the elements of said integrated circuit and routing said signal net, wherein said method comprises the step of branching (1b33, 1b34) an end line (2a2) if another end line (2a1) is branched (1b31, 1b32).

45. A method of placing and routing elements of a semiconductor integrated circuit as claimed in any one of claims 42 to 44, wherein said signal net is a clock signal net.

46. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 45, wherein said method includes the step of routing the signal net (MCN) along a reserved area (PDA).

47. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 45 or 46, wherein said method includes the step of calculating arrival time at each predetermined position in said signal net (MCN).

48. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 47, wherein said method includes the step of determining a width of each line in said signal net (MCN) so as to minimize the arrival time calculated at each predetermined position.

49. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 47, wherein said method includes the step of displaying the calculated arrival time in the vicinity of each predetermined position (1d1, 1d21, 1d22; 1c1, 1c2, 1c3, 1c4) on a screen (13) that displays said signal net (MCN).

50. A method of placing and routing elements of a semiconductor integrated circuit as claimed in claim 49, wherein the predetermined positions in said signal net (MCN) include branch points (1d1, 1d21, 1d22) and end points (1c1, 1c2, 1c3, 1c4) of said signal net.

51. An apparatus for placing and routing elements of a semiconductor integrated circuit, having an input unit (201) for entering data, a storage unit (203) for storing data, a processor (204) for placing and routing the elements of said integrated circuit according to data from said input unit and said storage unit, and a display unit (202) for displaying images according to data provided by said processor, wherein said apparatus comprises:

a means for picking out a signal net among the elements of said integrated circuit;

a means for extending or shortening one (2a1) of end lines when routing said signal net; and

a means for extending or shortening the other end lines (2a2; 2a2, 2a3) in response to the extension or shortening of said end line (2a1).

52. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 51, wherein said end lines (2a1, 2a2) are extended or shortened in response to a change in a capacitance or resistance of a line.

53. An apparatus for placing and routing elements of a semiconductor integrated circuit, having an input unit (201) for entering data, a storage unit (203) for storing data, a processor (204) for placing and routing the elements of said integrated circuit according to data from said input unit and said storage unit, and a display unit (202) for displaying images according to data provided by said processor, wherein said apparatus comprises:

a means for picking out a signal net among the elements of said integrated circuit;

a means for branching (1b31, 1b32) one (2a1) of end lines when routing said signal net; and

a means for branching (1b33, 1b34) another end line (2a2) in response to the branching of said end line (2a1).

54. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in one of claims 51 of 53, wherein said storage unit (203) comprises:

a means (231) for storing logic circuit information such as a net list;

a means (232) for storing routing attribute information to identify clocks and signals;

a means (233) for storing resource information such as information about the elements of said integrated circuit, and

a means (234) for storing programs such as sequences of processes.

55. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in one of claims 51 or 53, wherein said signal net is a clock signal net.

56. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 55, wherein said signal net (MCN) is routed along a reserved area (PDA).

57. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 55, wherein an arrival time at a predetermined position in said signal net (MCN) is calculated.

58. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 57, wherein a width of each line in said sig-

nal net (MCN) is determined to minimize the arrival time calculated at each predetermined position.

59. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 57, wherein said calculated arrival time is displayed in the vicinity of each predetermined position (1d1, 1d21, 1d22; 1c1, 1c2, 1c3, 1c4) on a screen (13) that displays said signal net (MCN).

60. An apparatus for placing and routing elements of a semiconductor integrated circuit as claimed in claim 59, wherein the predetermined positions in said signal net (MCN) include branch points (1d1, 1d21, 1d22) and end points (1c1, 1c2, 1c3, 1c4) of said signal net.

Fig.1  
(Prior Art)

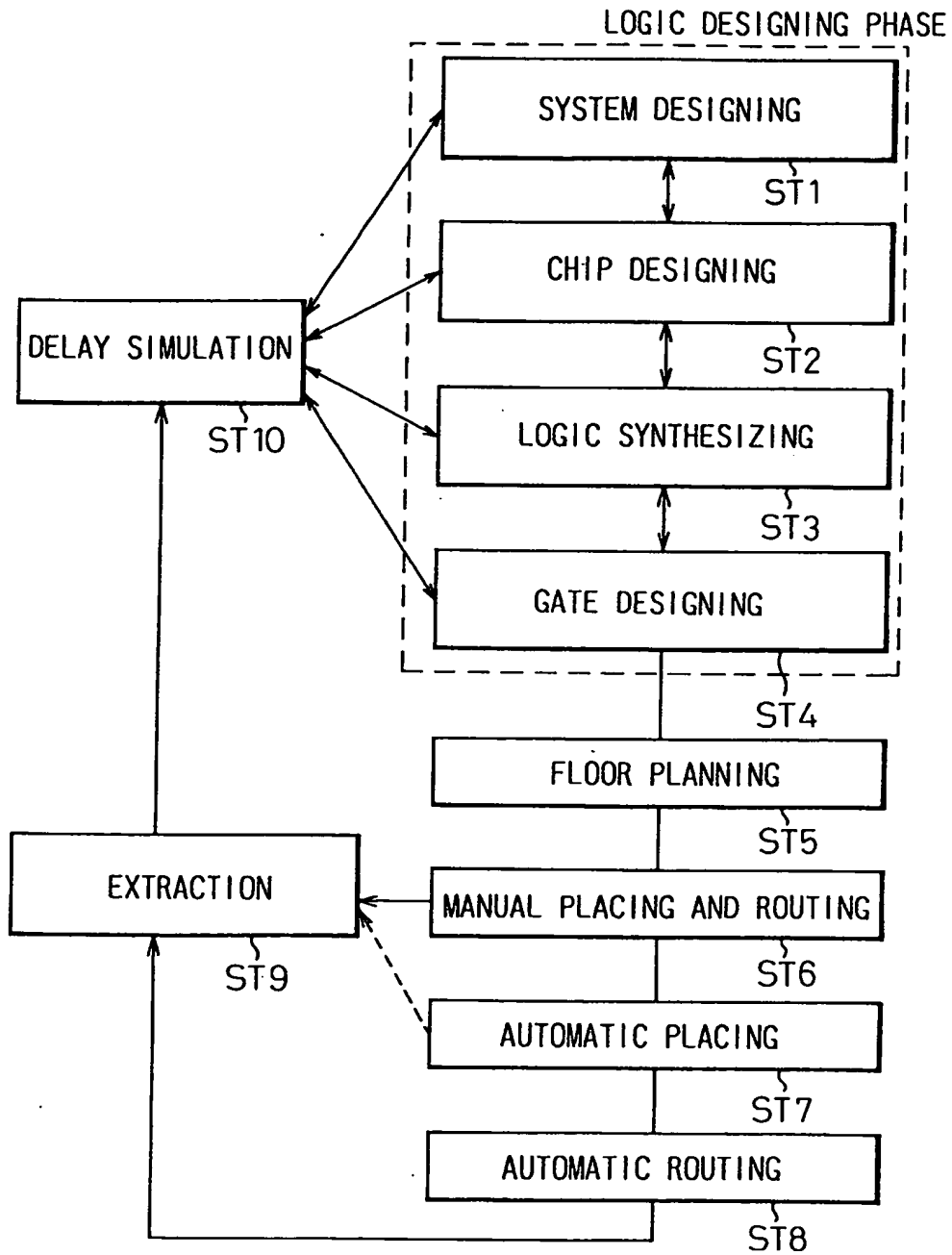


Fig. 2

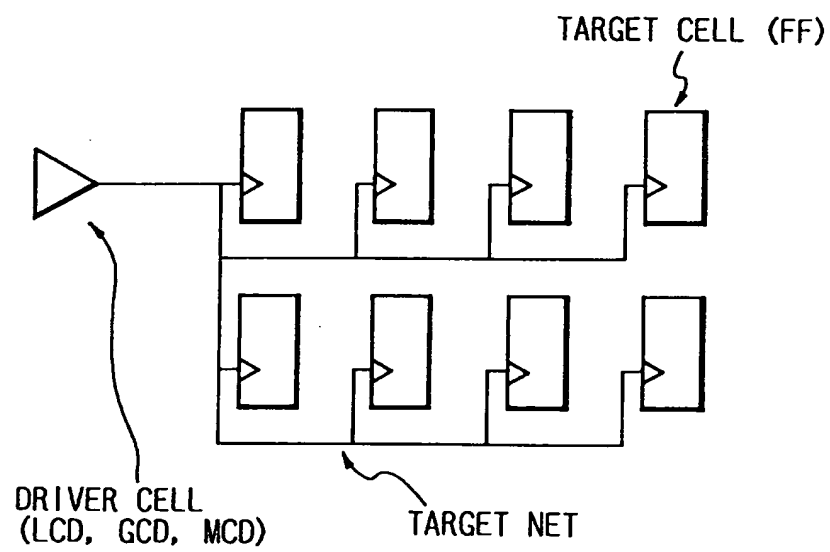


Fig. 3

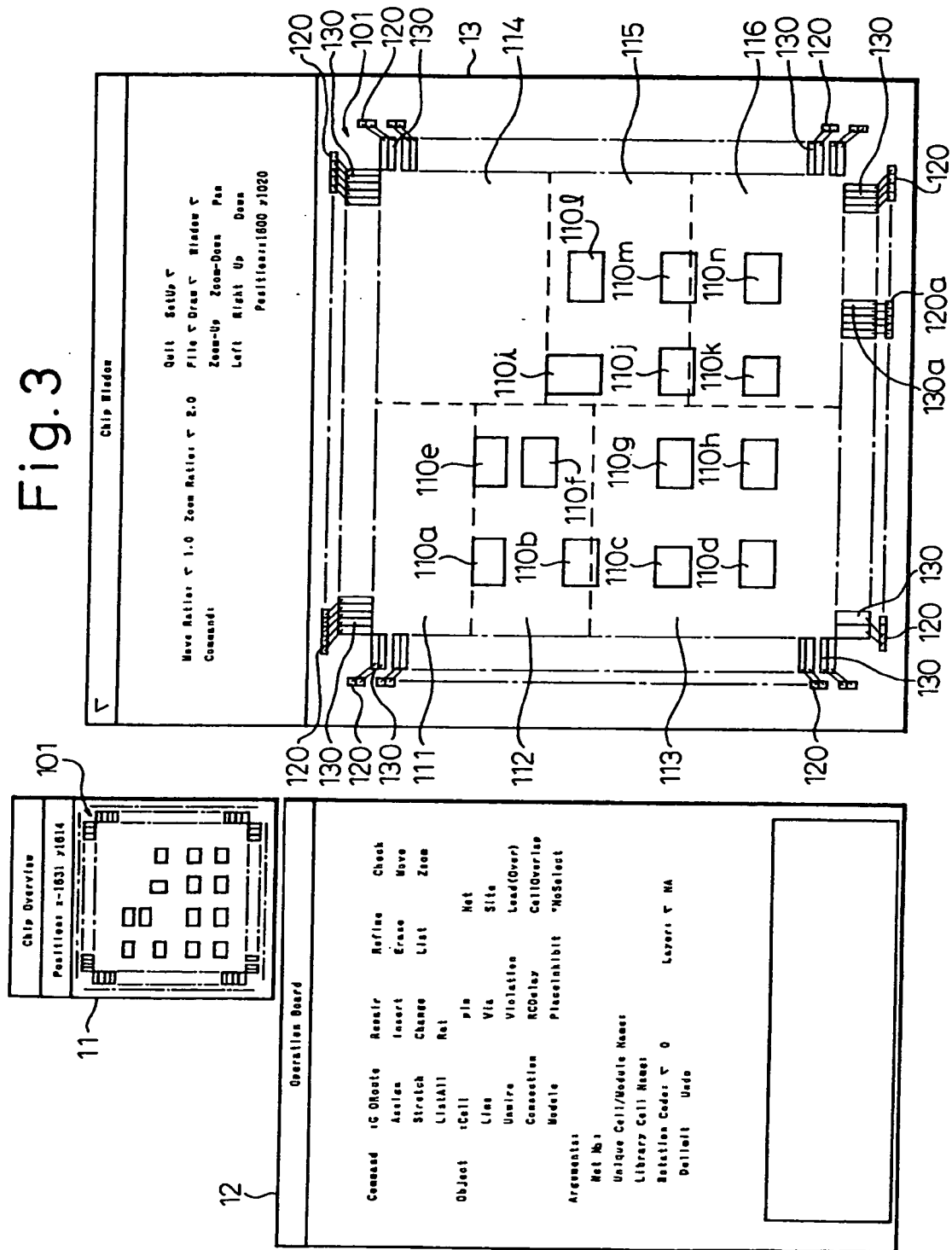
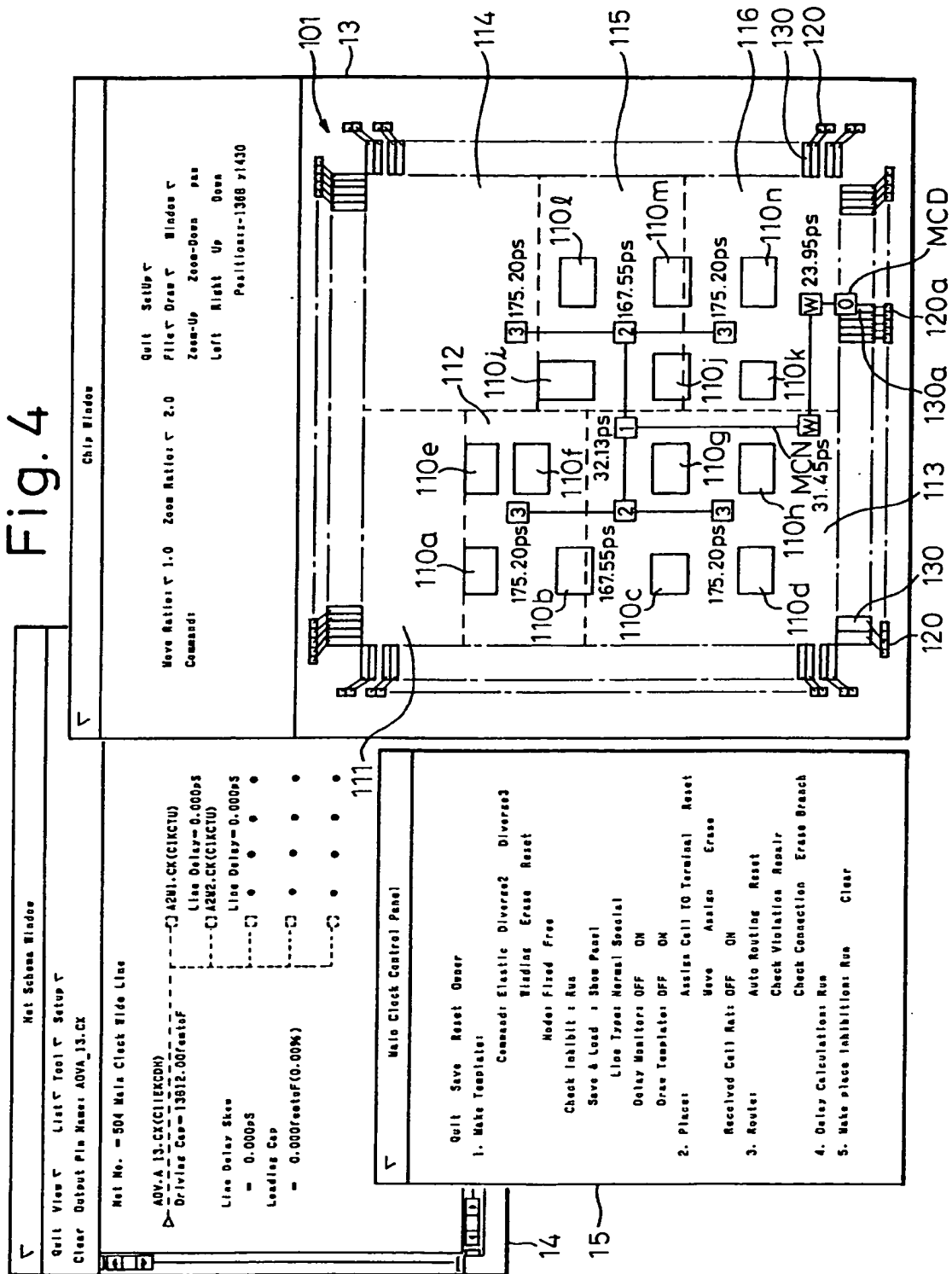


Fig. 4



உதிர்த்

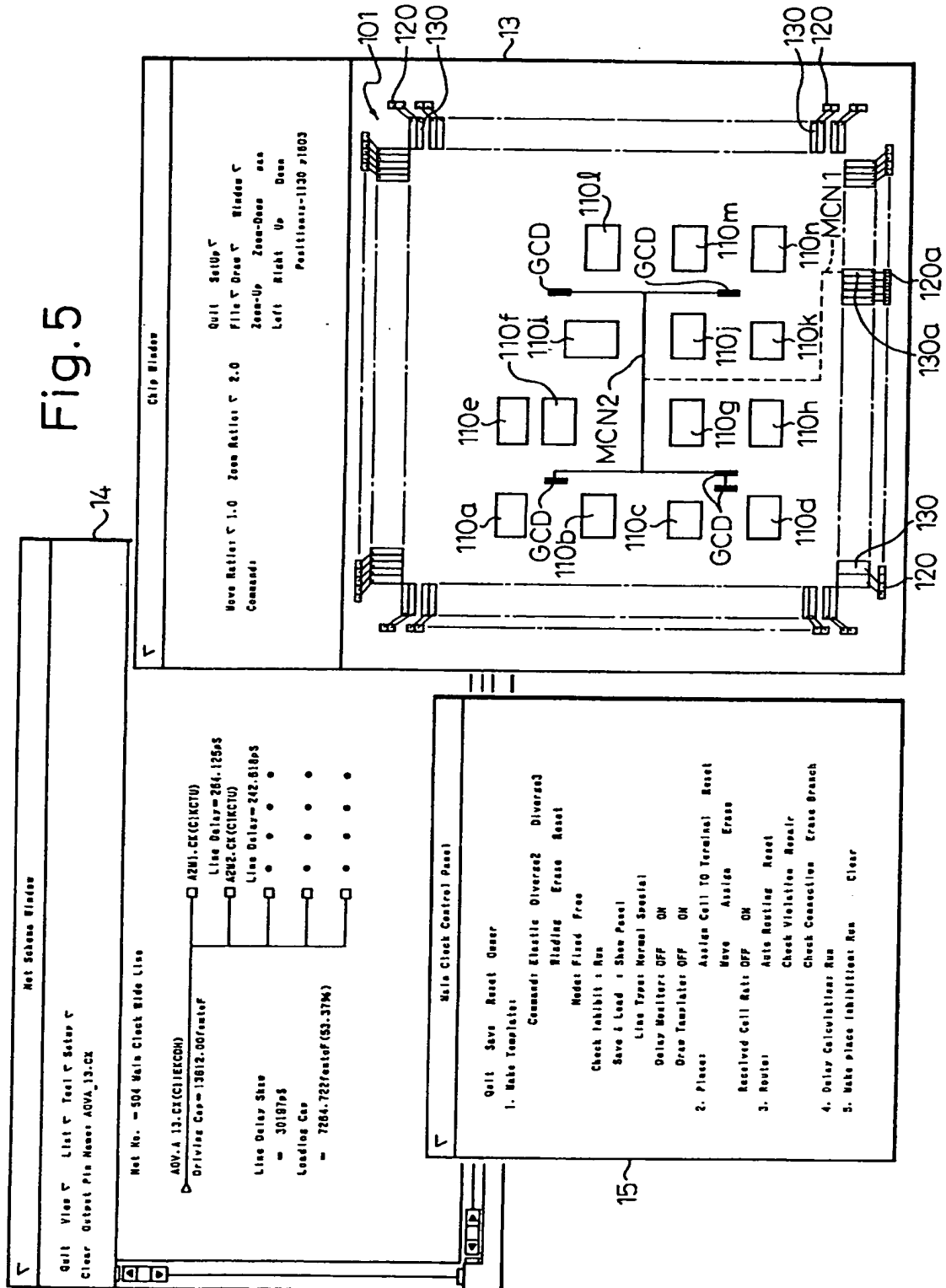


Fig. 6

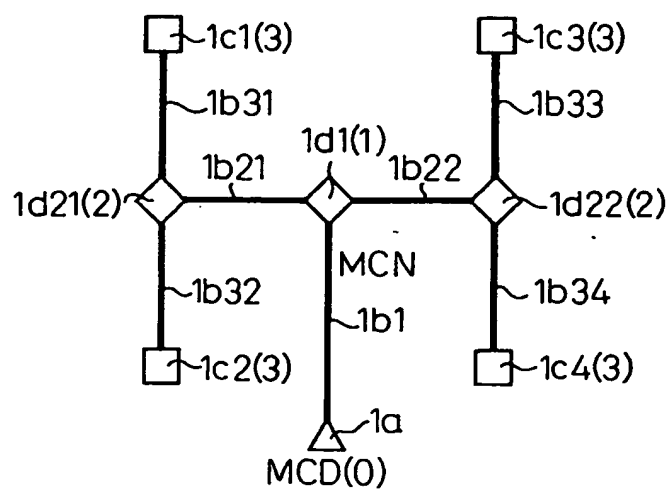


Fig. 7

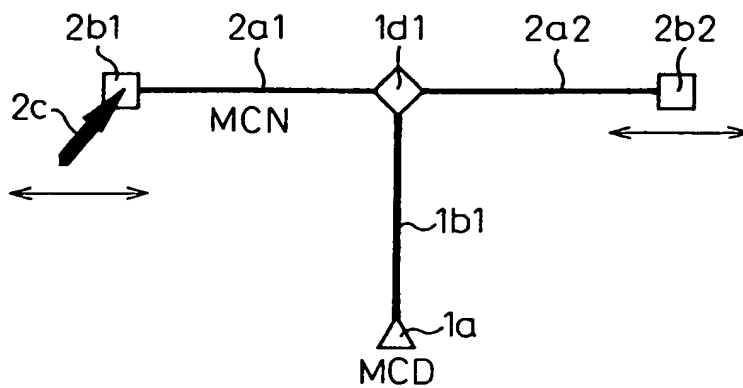


Fig.8

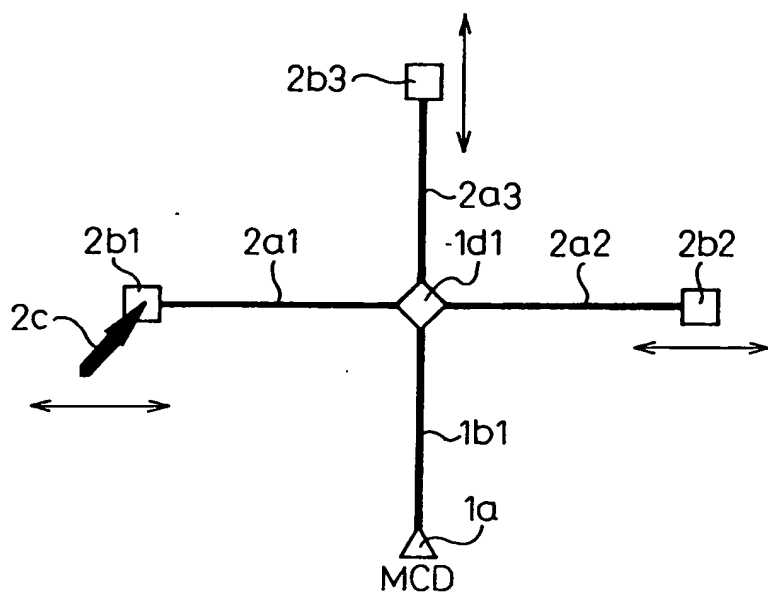


Fig.9

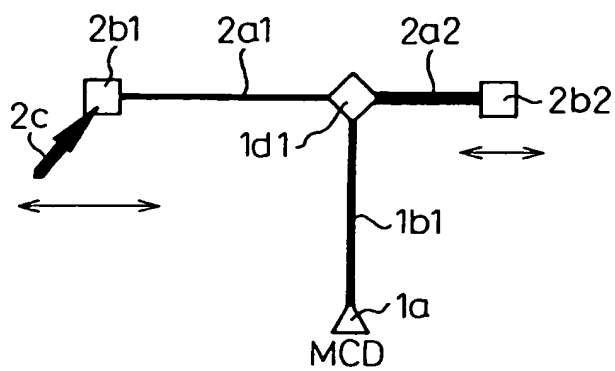


Fig.10

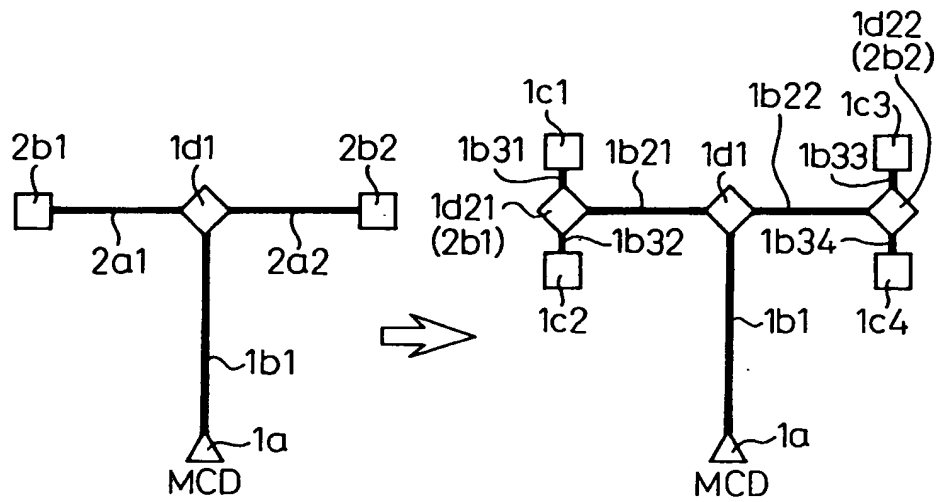


Fig.11

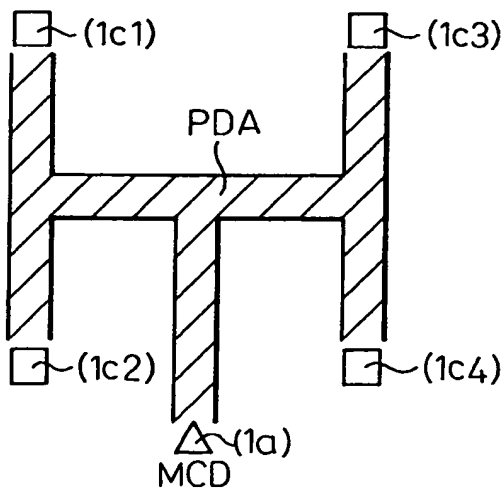
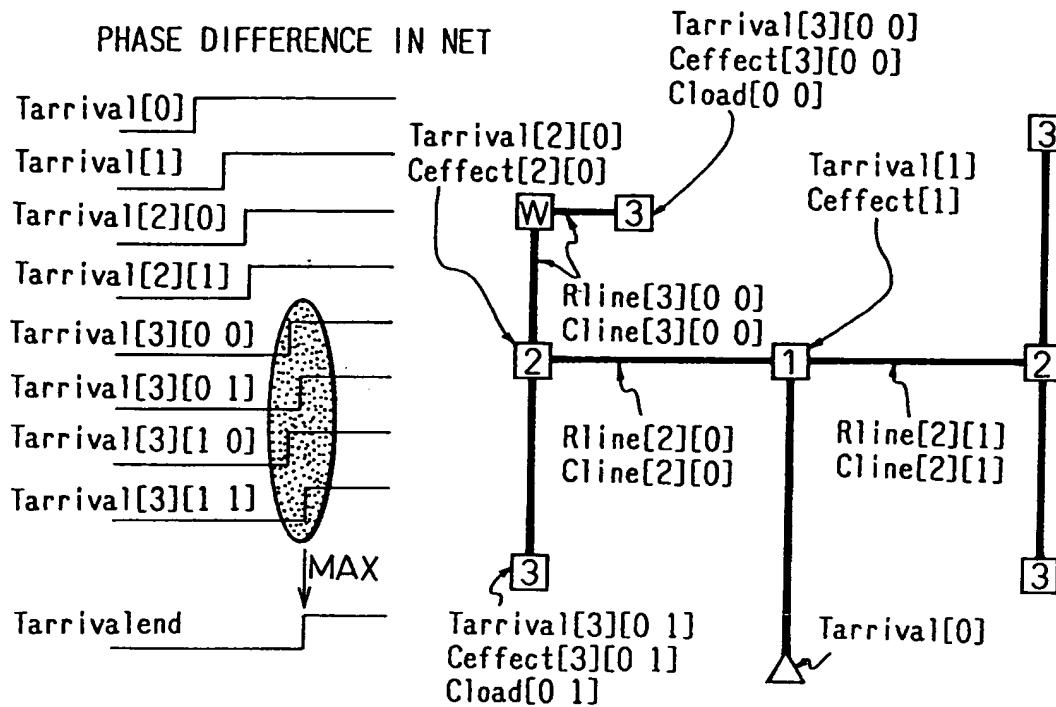


Fig.12



ARRIVAL TIME AT TERMINAL  
 $Tarrival_{end} = \text{MAX}(Tarrival[n])$

$n = 3$

$$\begin{aligned}
 Tarrival[3][i\ j] &= Rline[3][i\ j] \times (Ceffect[3][i\ j] \\
 &\quad + Cline[3][i\ j]/2) + Tarrival[2][i] \\
 Tarrival[2][i] &= Rline[2][i] \times (Ceffect[2][i] \\
 &\quad + Cline[2][i]/2) + Tarrival[1] \\
 Tarrival[1] &= Rline[1] \times (Ceffect[1] \\
 &\quad + Cline[1]/2) + Tarrival
 \end{aligned}$$

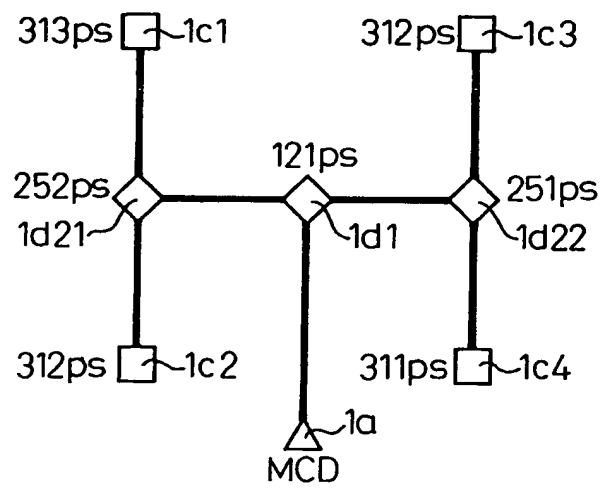
$$\begin{aligned}
 Ceffect[3][i\ j] &= Cload[i\ j] \\
 Ceffect[2][i] &= \sum (j, Cline[3][i\ j]) + \sum (j, Ceffect[3][i\ j]) \\
 Ceffect[1] &= \sum (i, Cline[2][i]) + \sum (i, Ceffect[2][i])
 \end{aligned}$$

$n$ : DEPTH OF TREE

$i, j$ : THE NUMBERS OF  
 BRANCHES

$Rline[n]$  AND  $Cline[n]$  ARE  
 CALCULATED FROM LINE  
 LENGTH BETWEEN BRANCHES,  
 OR BETWEEN BRANCH AND  
 TERMINAL

Fig.13



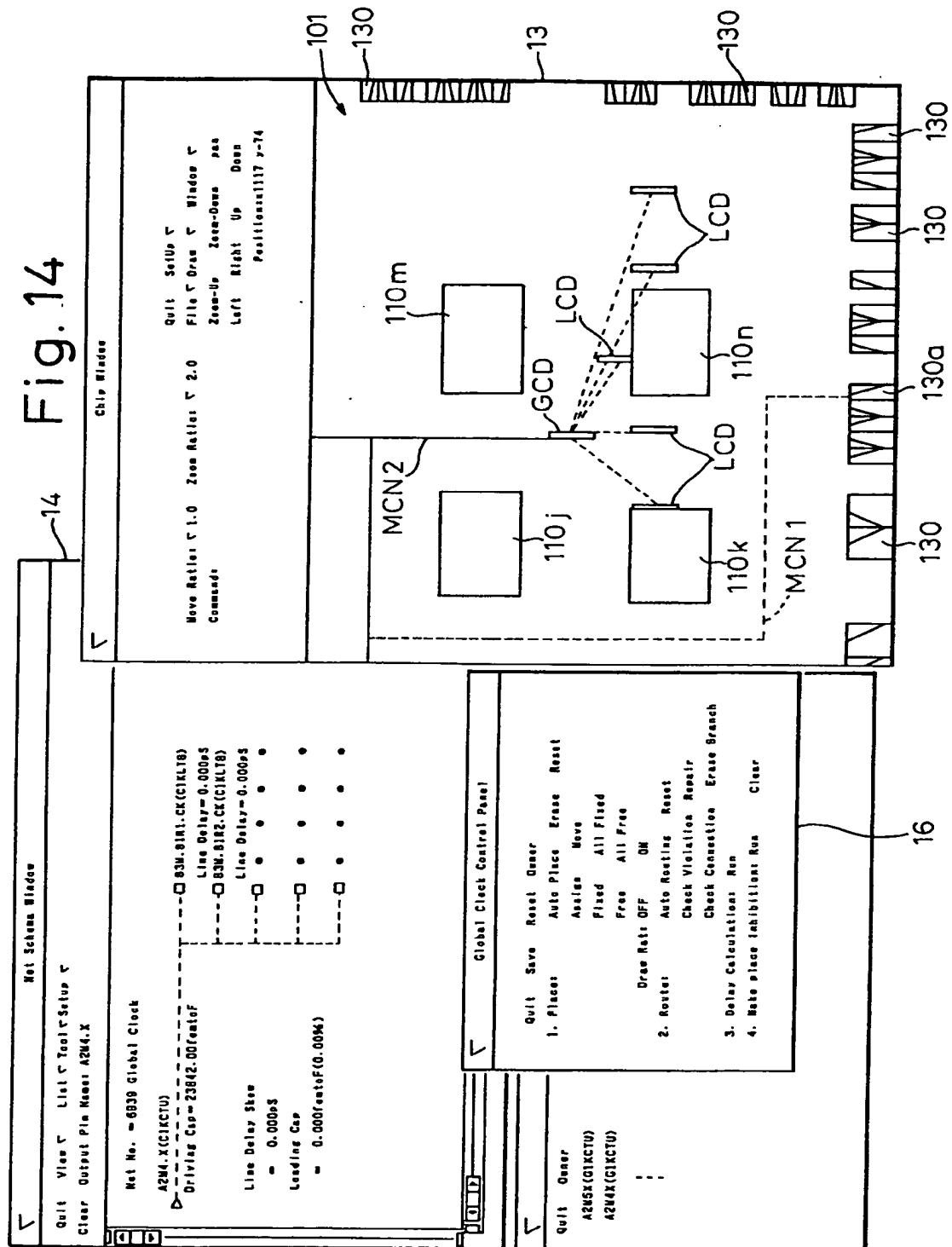


Fig.15

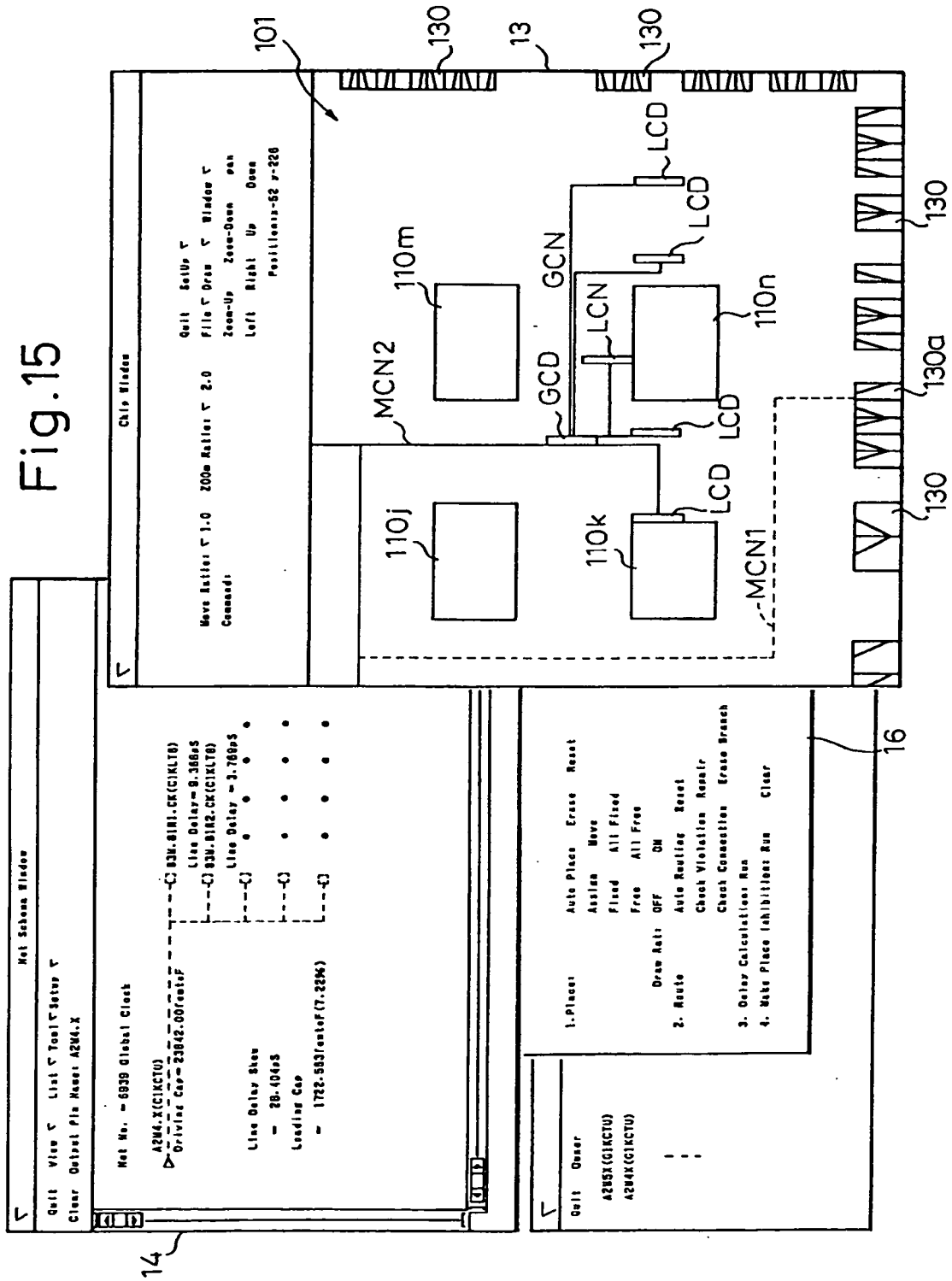


Fig. 16

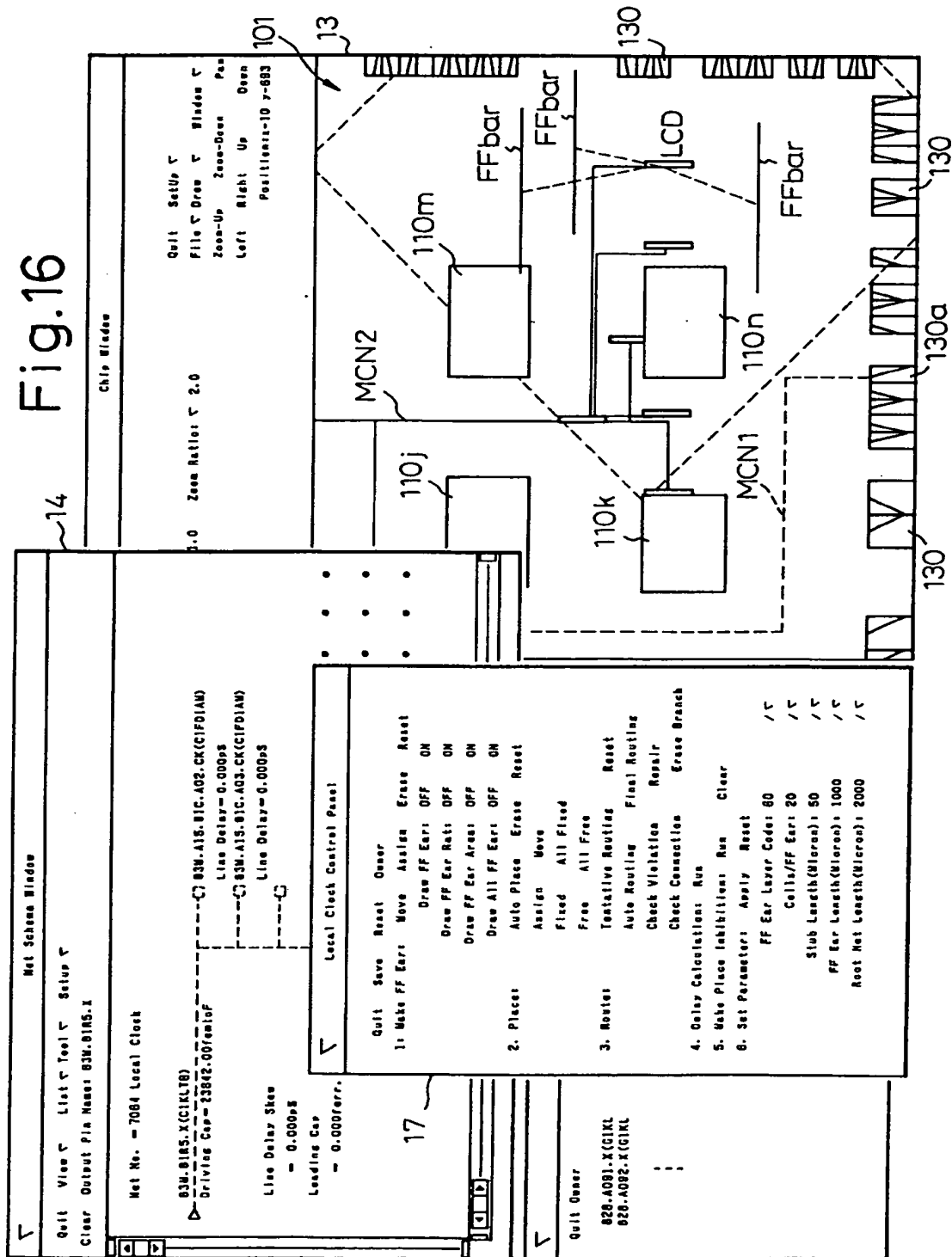


Fig. 17

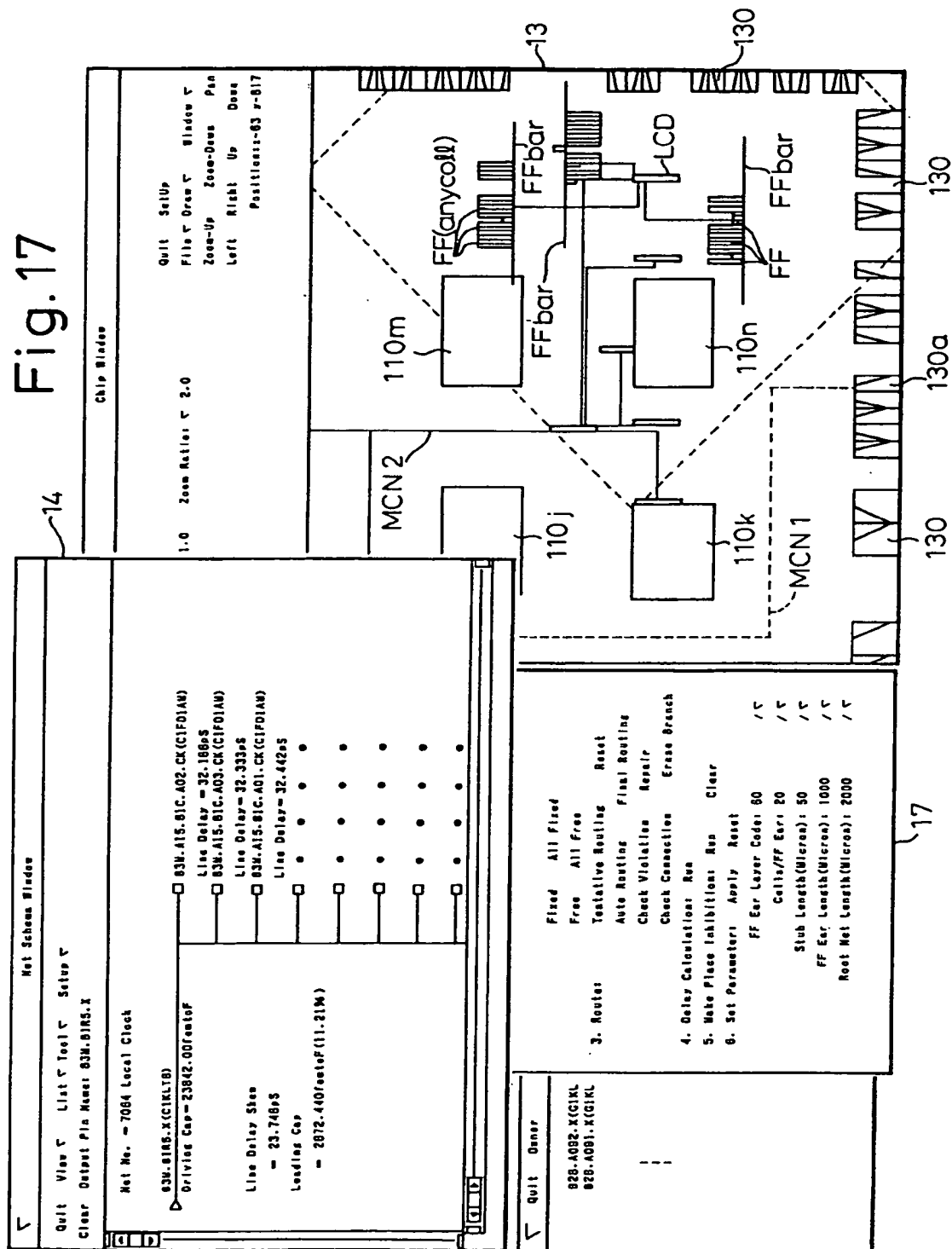


Fig. 18

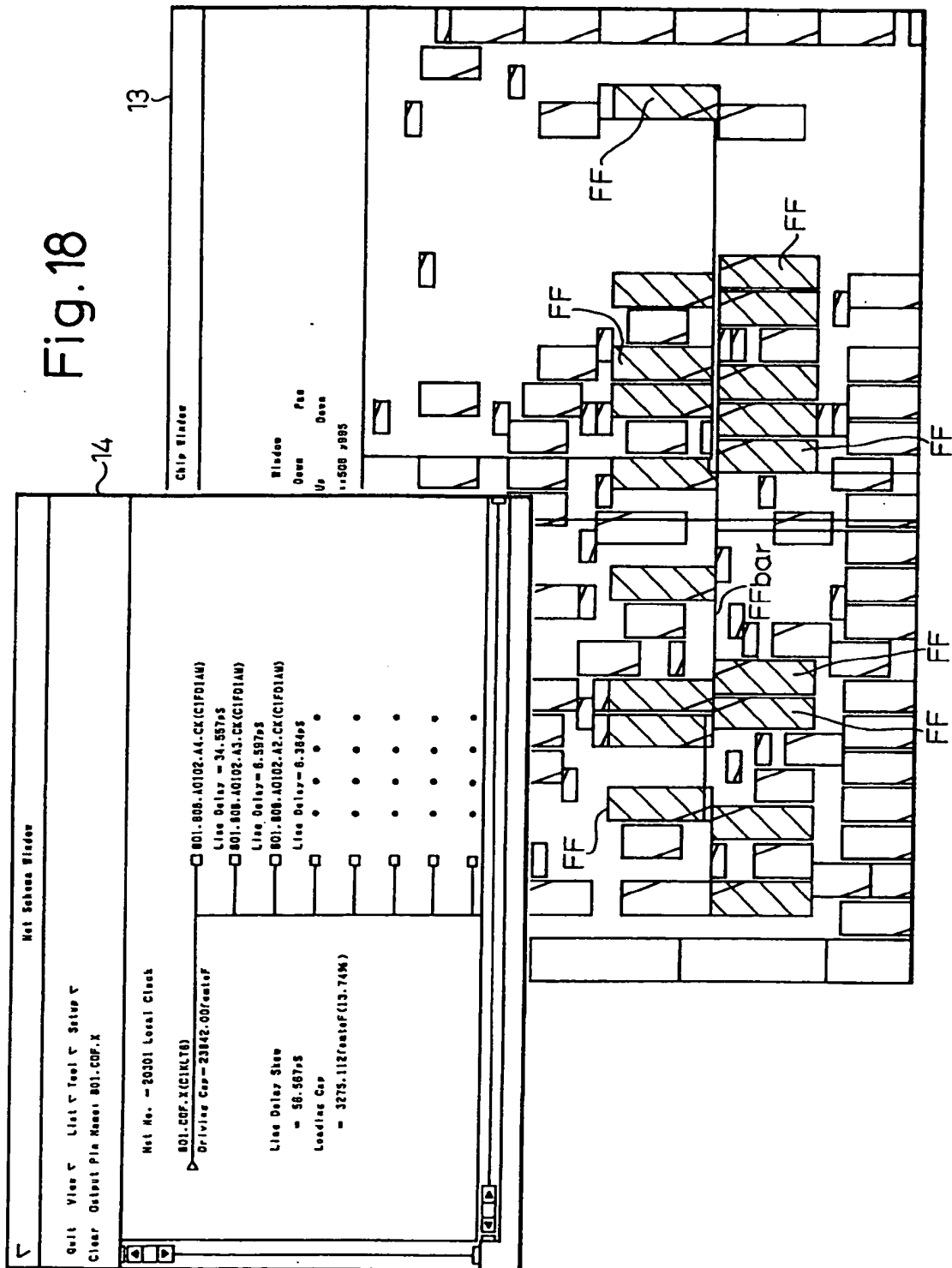


Fig.19

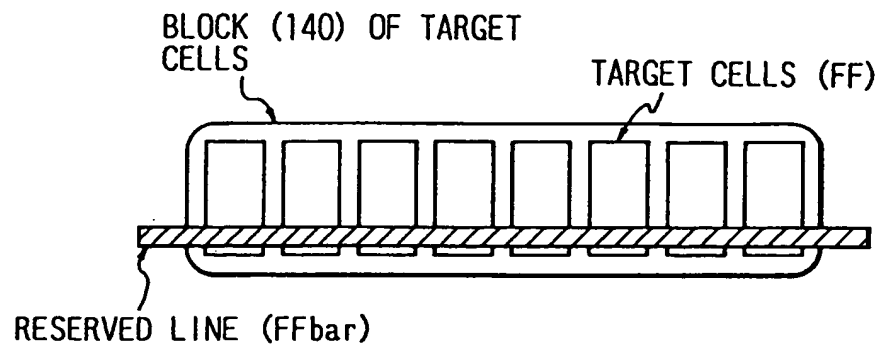


Fig. 20

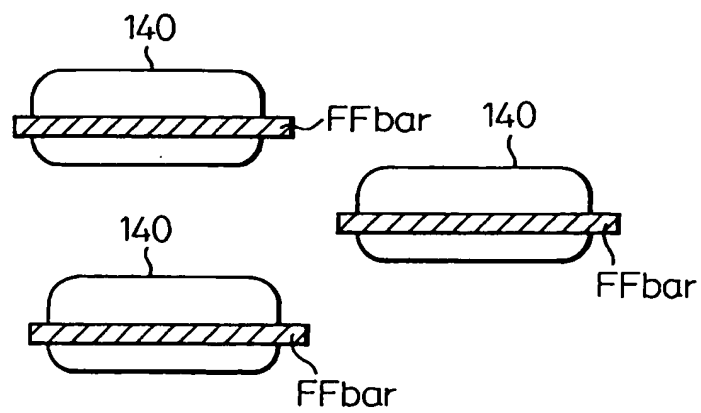


Fig.21

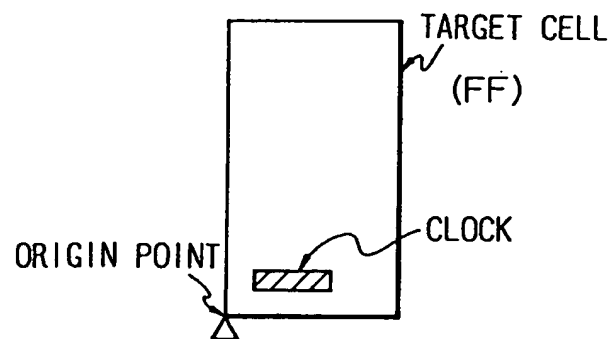


Fig. 22

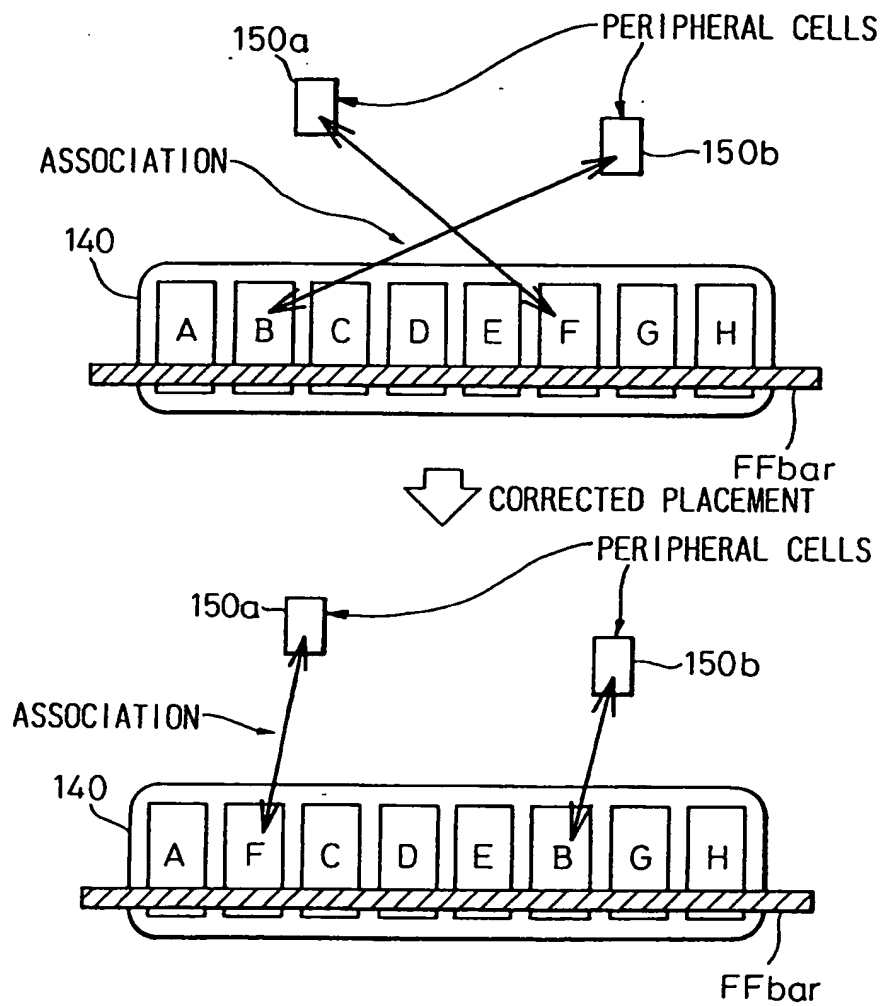


Fig. 23

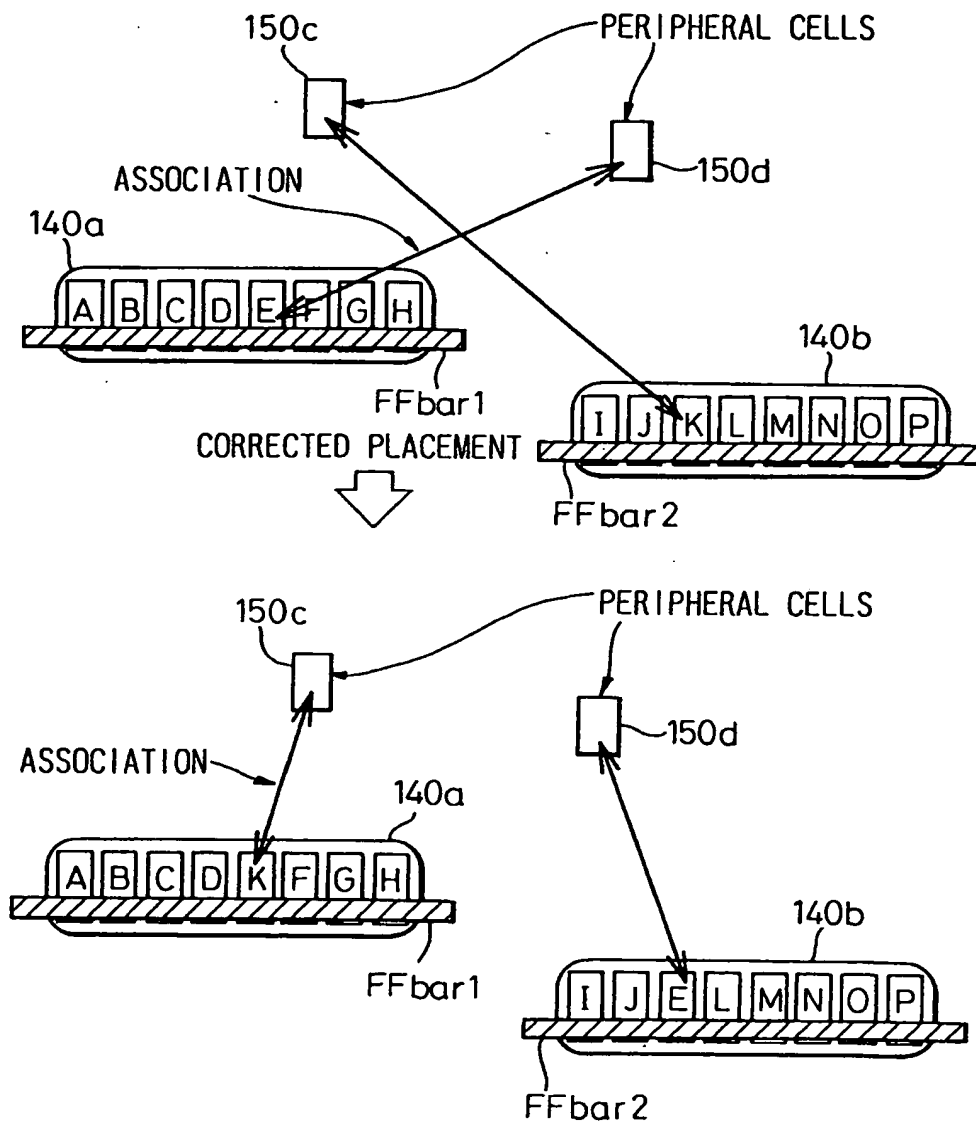


Fig. 24

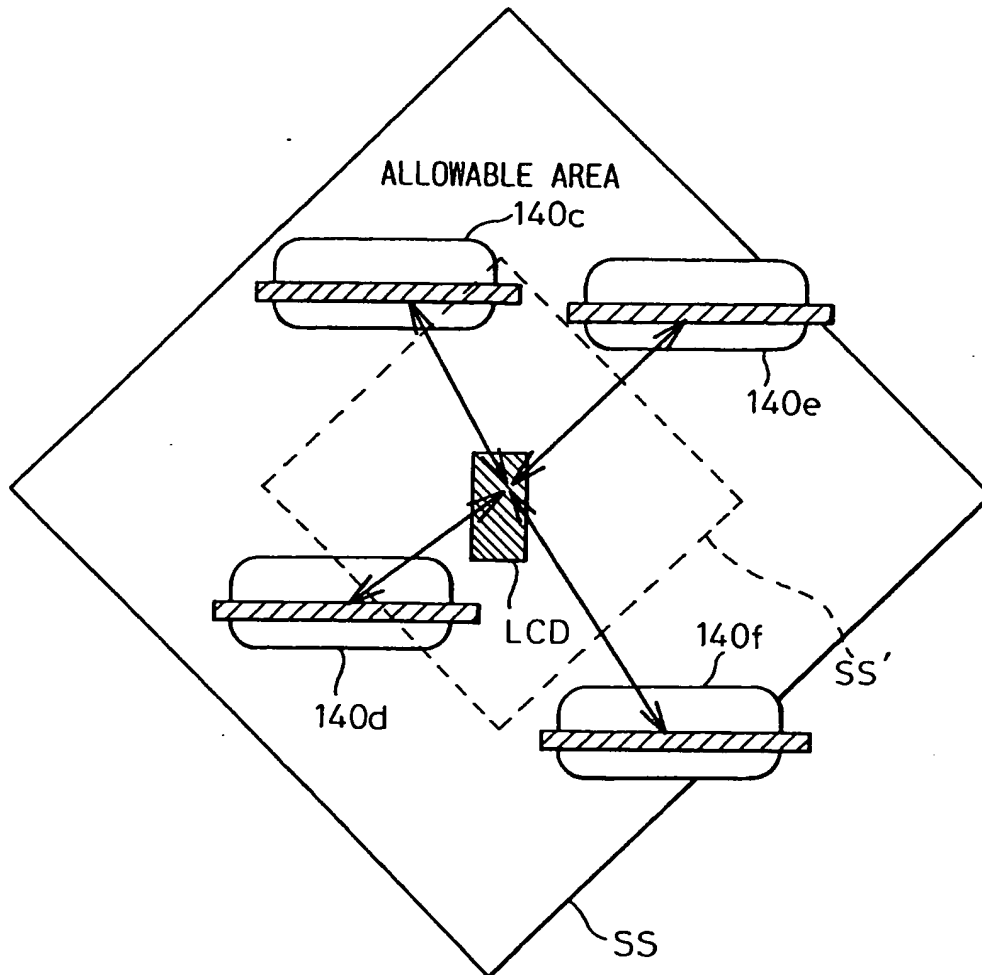


Fig. 25

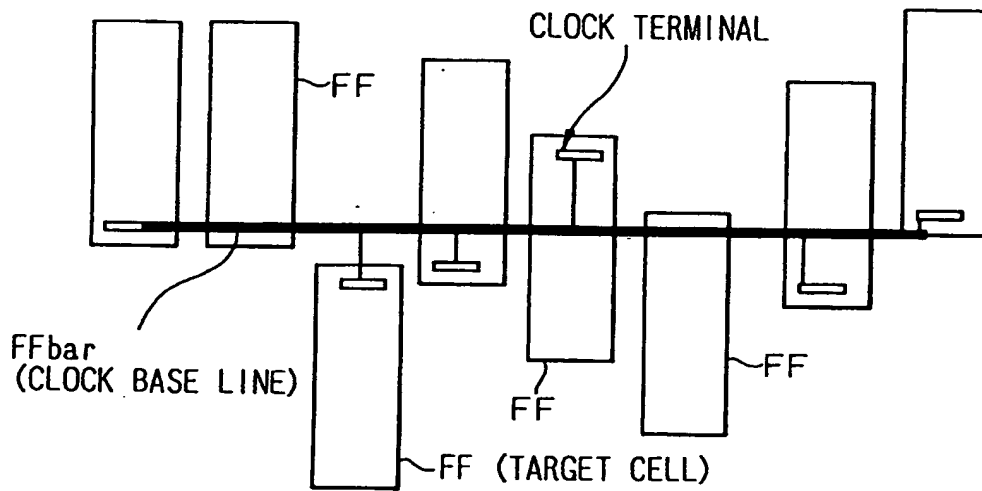


Fig. 26

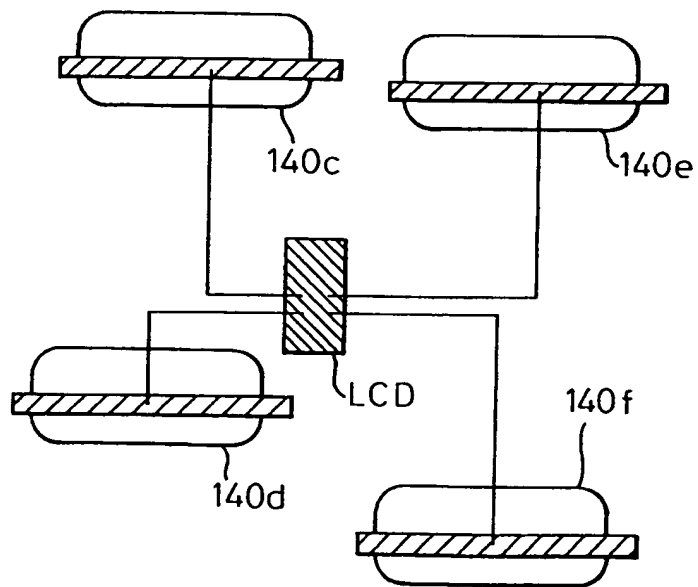


Fig.27

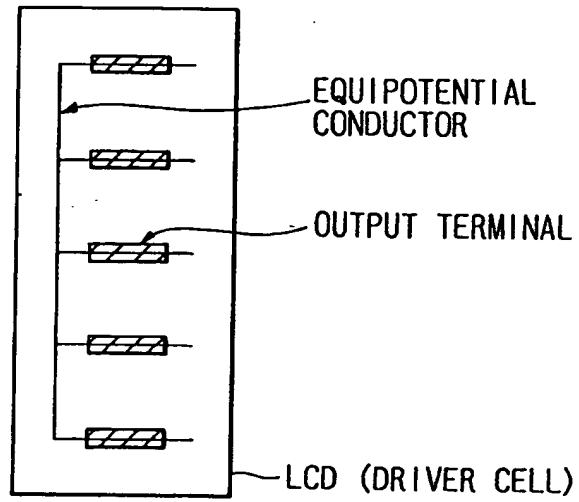


Fig.28

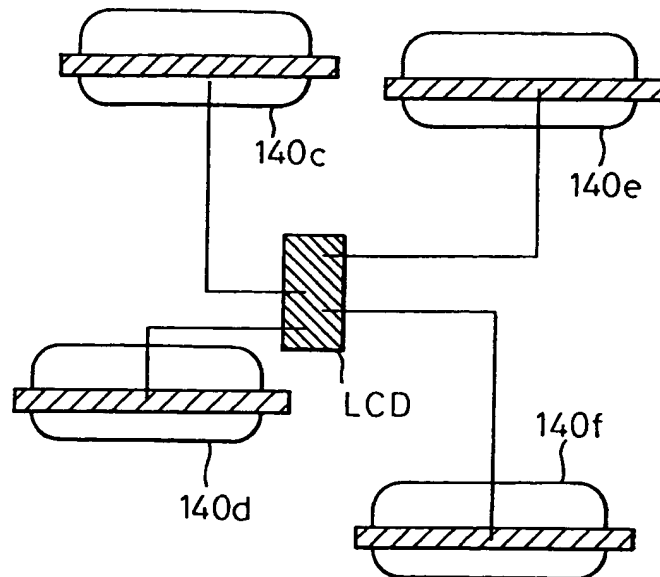


Fig. 29

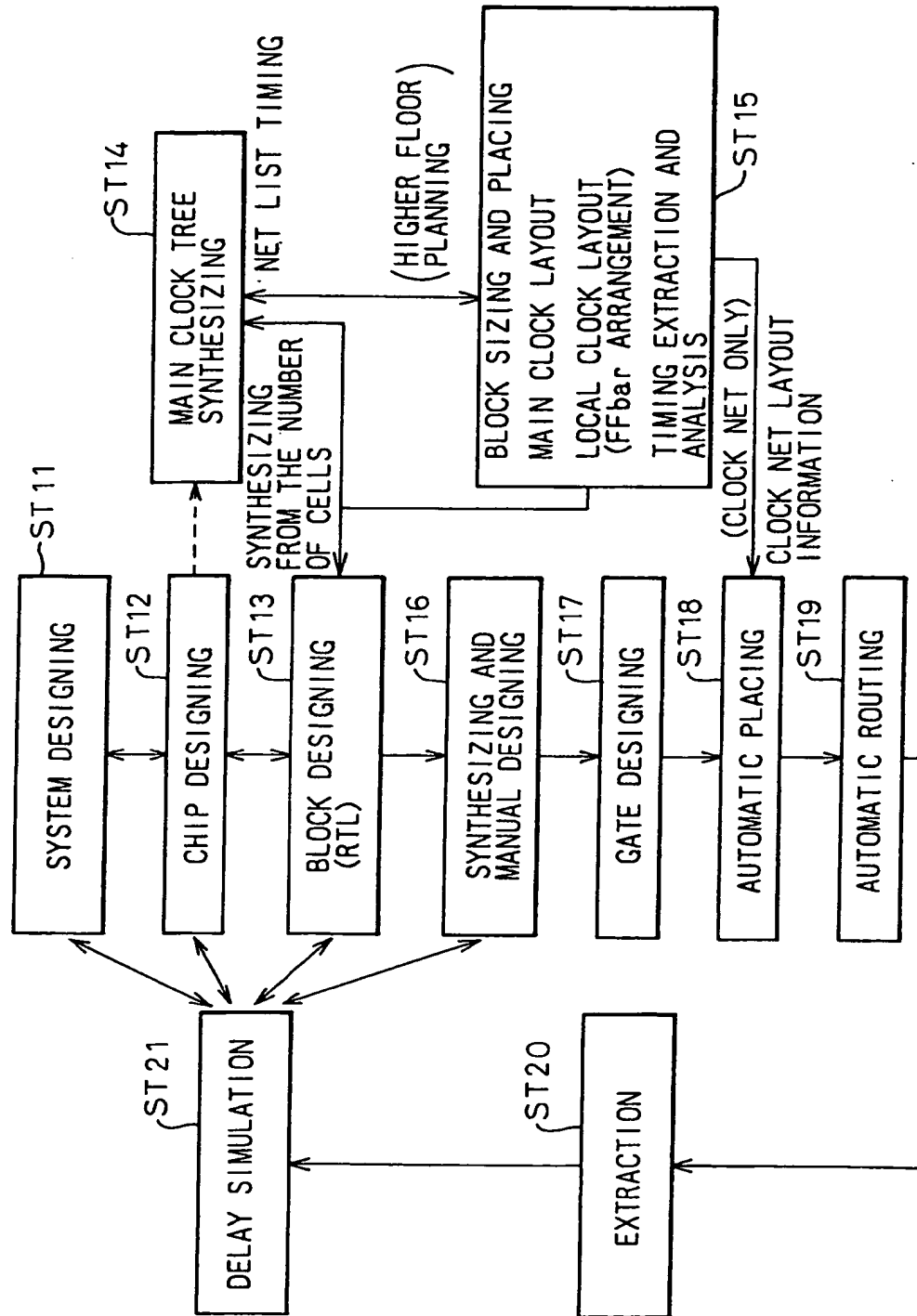


Fig. 30A

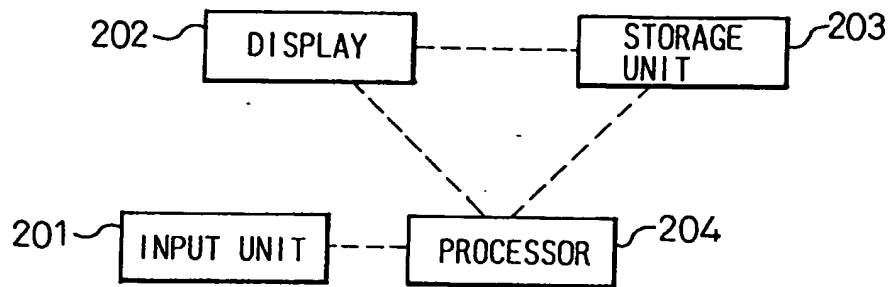


Fig. 30B

